Summary

This is a general description of a dynamic HVDC model designed to be used in cooperation with the load flow model introduced in the PSS/E program version 26.2 (Power System Simulator, PTI - Power Technologies, Inc.).

The main goal of the report is to show how to use these detailed DC Transmission models and with emphasis on how to run it. The load flow model is available from PTI and the dynamic model is available from ABB Power Systems.

The HVDC models are designed to operate either as a Line Commutated Converter (LCC) or as a Capacitor Commutated Converter (CCC) as well as line/cable transmission or as a back-to-back transmission. The selection of transmission type is done, by setting parameters in the indata files.

The dynamic HVDC model simulates all the electrical equipment of a monopolar HVDC Transmission including the two converter stations as well as all the basic control functions. The only exception is the ac filters, which must be included externally in the load flow setup. The data of the electrical equipment and the parameters of the control functions are determined by the data in a special indata file.

Calculation of the model parameters and the operational procedure are presented in Appendix 1. An actual HVDC Back-to-Back Transmission system with capacitor commutated converters has been setup with reduced ac networks All the system parameters has been calculated and introduced as input data to the PTI load flow model and also as input to ABB's Dynamic Model in PSS/E.

Table of Contents

1 INTRODUCTION

Recent years have seen growing demands of advanced simulation tools to investigate electrical power systems worldwide. These demands have focused the interest on the digital simulation techniques for analysis of the dynamics of power systems. Several power utilities have requested an accurate model of an HVDC transmission, which can be used at dynamic simulations of electromechanical transients. ABB can now present detailed HVDC models to be used in different types of simulation programs like PSS/E and Simpow.

This report presents detailed models to be used in the PSS/E digital simulation programs. The models can be used both for conventional line commutated converters and capacitor-commutated converters.

These models were written basically to attend the needs of many customers that already use the PSS/E program and wish to have a detailed representation of an HVDC Transmission, while performing dynamic studies on their networks.

This report describes the setup and operation procedure from the load flow calculation to the setup of the dynamic HVDC Model equipped with CCC converters.

The advantages of the CCC concept have been employed to create a stable system capable of transferring power at low short circuit ratio. The reactive power generation and consumption vary with the active power load of the dc link. The magnitudes of load rejection overvoltages are reduced due to the lower residual reactive power generation at load rejection.

The load flow model of PSS/E has been enhanced to accommodate capacitor commutated converters and it has been included in version 26 of the PSS/E program. Power Technologies Inc. (PTI) has designed the model with support from ABB Power Systems AB. The dynamic models for dc transmission with one or both represented as capacitor commutated converters are not included in the standard model library but is available at ABB Power Systems.

To create a complete model of the transmission system, an application of a 1100 MW monopolar transmission block has been presented in the appendix at which the setup procedure is discussed. The complete system is set up in both the load flow program and in the dynamic simulation. The parameters of the standard model in the load flow program and the corresponding dynamic model have been derived.

2 FUNCTIONAL DESCRIPTION OF HVDC MODEL

2.1 HVDC Equipment

An application with a back-to-back transmission has been used as reference for the design of a load flow model and a dynamic model in the simulation program PSS/E.

The substation is designed according to the new principles presented in the concept HVDC 2000. A compact design is obtained by a combination of the following equipment,

- commutation capacitors
- continuously tuned ac filters

A general introduction to the CCC-concept is presented in the paper CIGRE 1996:14-ref[3]

A detailed description of the concept is presented in the report “The concept for capacitor commutated converter stations”, ref[1].

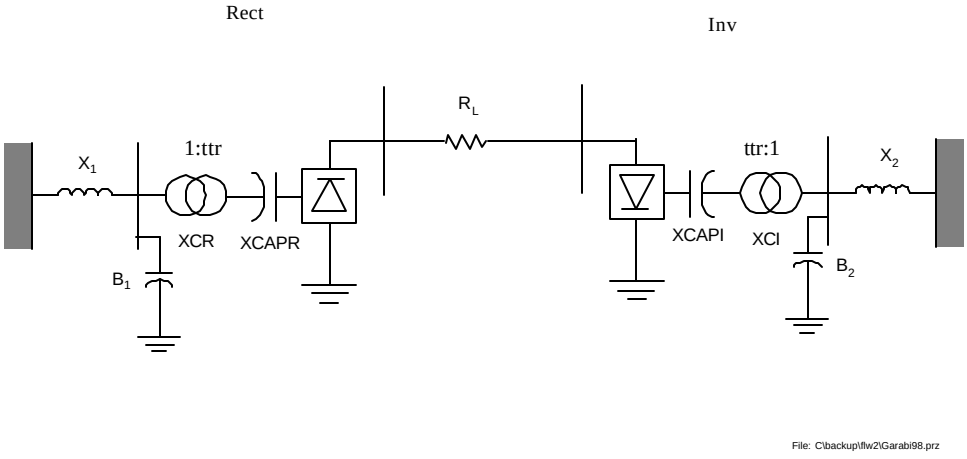
The CCC converters can be operated in systems with effective short circuit ratios (ESCR) as low as 1.0. The CCC-concept also provides better stability and reduces the need for shunt reactive power support as compared to the conventional converter design.

The HVDC 2000 concept may also include automatically tuned ac filters, ConTune. A filter in which tuning is automatically adjusted to follow frequency variations and component variations. The filter can be designed with high Q-factor to provide low impedance for the harmonics. Automatic tuning will also ensure that the risks of resonance and current amplification phenomena are eliminated and the ac filter component ratings can be reduced. Proposed filters are 11th, 13th, 24th and 36th harmonic filters

2.2 HVDC Load Flow Model

The TWO-Terminal DC Transmission model is included in an ac network system as a HVDC model representing a line or cable transmission configuration as well as a back-to-back configuration. The dc side of the transmission is only represented by a dc resistor.

PSS/E Load Flow Model



The 12-pulse converter bridge consists of two series connected 6-pulse bridges.

The converter bridge can be connected as conventional or series capacitor commutated converters.

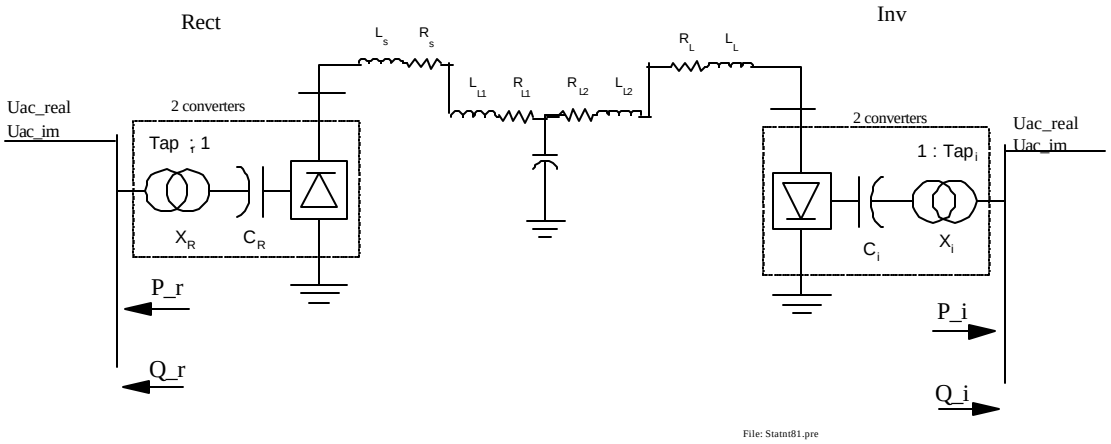
The load flow standard model, 'Two-Terminal DC Transmission', in the PSS/E program uses only a resistor representing the dc side and the same model is thus used for both line and back-to-back transmissions.

2.3 HVDC Dynamic Model

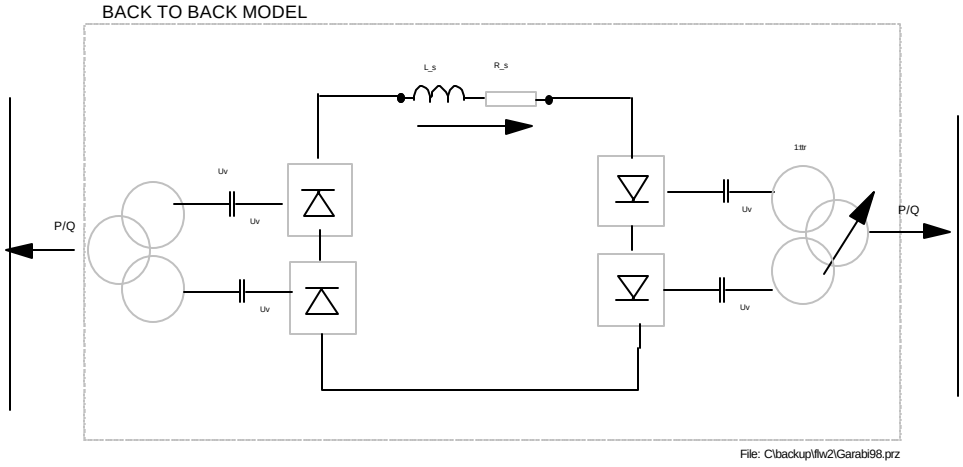
2.3.1 Dynamic model configuration

A dc line or dc cable transmission is represented by a dynamic model of following configuration. The converter model could represent one or several series connected groups.

LINE/CABLE MODEL



A back-to-back transmission is represented by a dynamic model of following configuration.



The same dynamic model, CDCAB2, can be used for both transmission configurations by setting the appropriate constants in the data file according to the data sheet.

2.3.2 Control Function

This paragraph describes only the main control functions. A more detailed description of the ABB control functions is included in the PSS/E manual of the non-standard model, see model description of CDCAB1, ref [5]

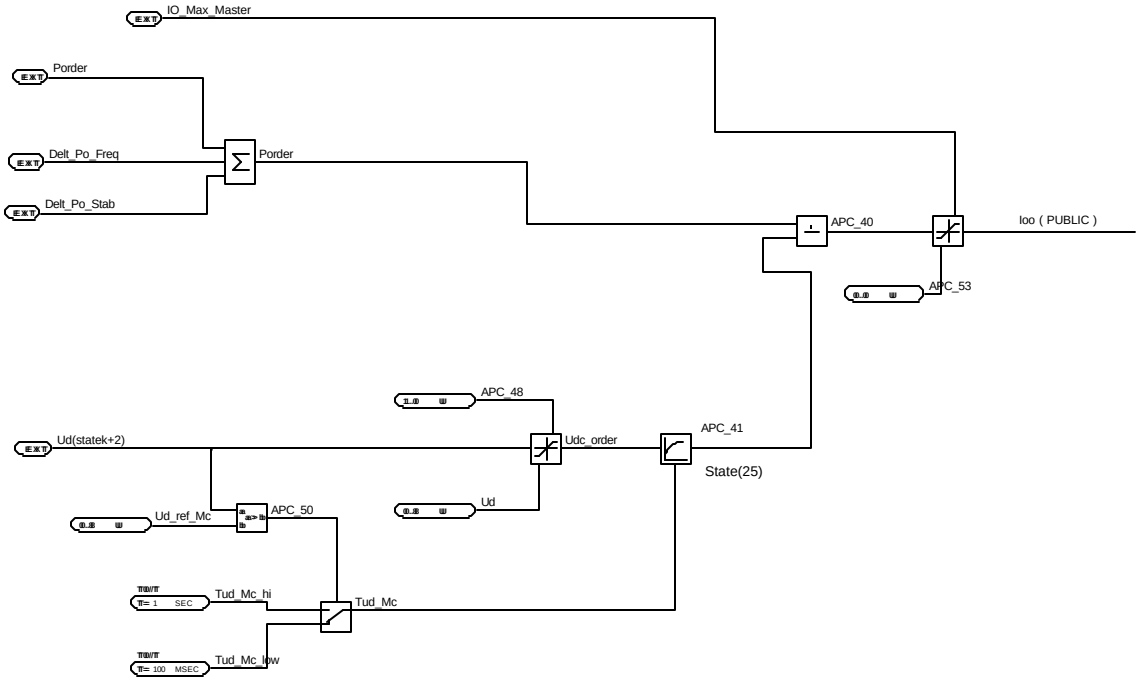
The control can be divided into following parts, a common Master controller controlling the transmitted power and for each converter there are the Current Order Limiter (COL), Current Control Amplifier (CCA) and Converter Firing Controller (CFC).

2.3.2.1 Master Control

The HVDC control functions can be divided into two parts, Master Control and Converter Control. The Master Control provides all the functions common for both converters and includes Active Power Control, Frequency Control and Damping Control.

Active Power Controller

The power controller calculates a reference value of the current order to the converters in the HVDC block according to the following diagram.



The Master Controller operates in two different modes, Constant Current control and Constant Power Control.

In the Power Control mode the contribution from Frequency Controller and the Damping Controller are added if the functions are activated and the total power order is determined according to:

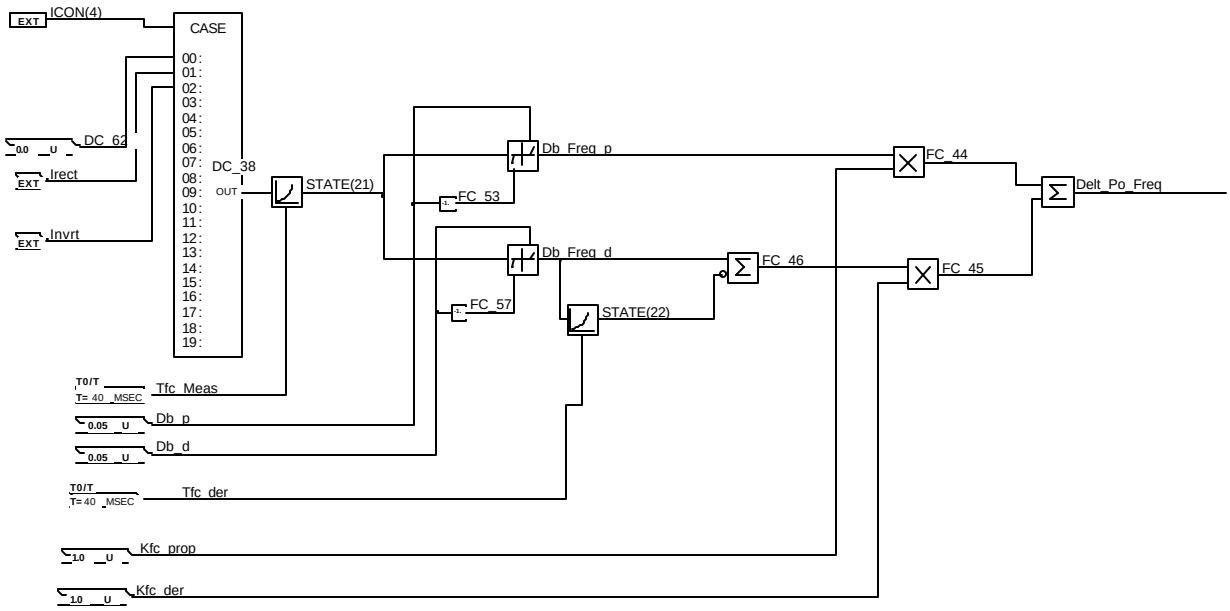
Power Order = Porder + Delt_Po_Freq + Delt_Po_Stab

The current order is calculated as

I order = Power Order / Udc_filter = Porder / State(k+25)

Frequency Controller

The Frequency Controller is designed as a PD-regulator with the proportional and derivative gains set by the parameters according to the diagram below. The input signal must exceed a deadband before the dc power is affected.



The frequency deviation of rectifier or inverter is selected as the input. At the frequency increase the controller adds a contribution to the power order if the rectifier is selected and reduces the power order if the inverter is selected.

The measured frequency is selected according to the control signal ICON(4) as,
If ICON(4) equal to 1

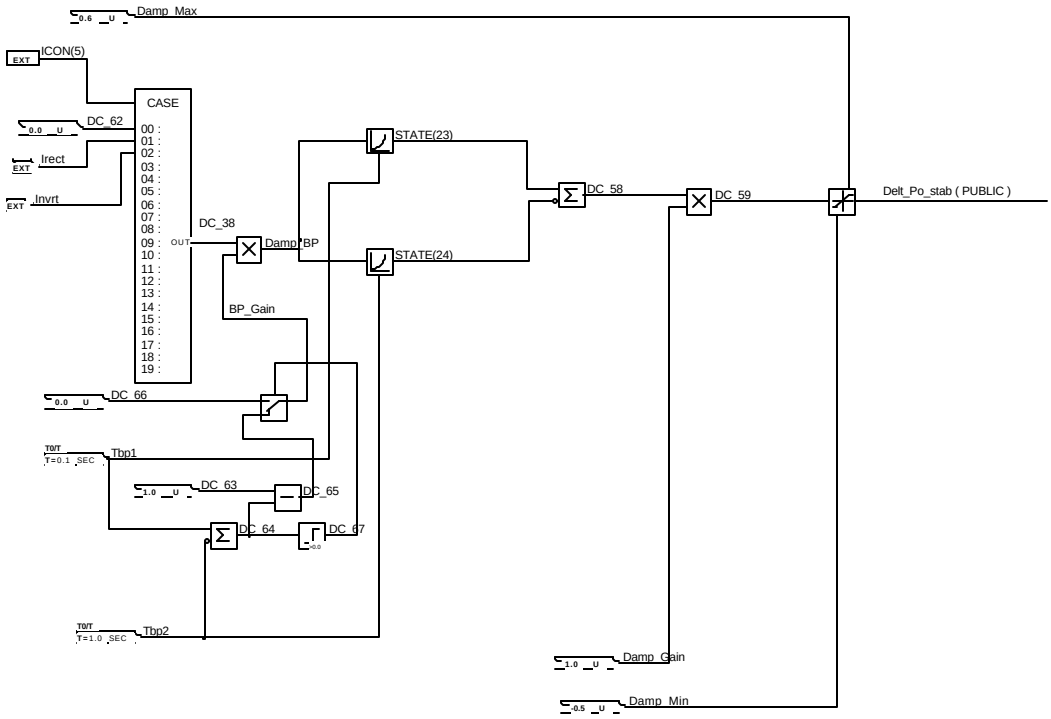
Bus voltage rectifier Freq_r = BSFREQ(Irect) * Freq_Nom_r

If ICON(4) equal to 2

Bus voltage inverter Freq_i = BSFREQ(Invrt) * Freq_Nom_i

Damping Controller

The Damping Controller is designed as a bandpass filter with the time constants Tbp1 and Tp2 according to the diagram below.



The frequency of rectifier or inverter is selected. At frequency increase the controller adds a contribution to the power order if the rectifier is selected and reduces the power order if the inverter is selected.

The measured frequency is selected according to the control signal ICON(5) as,

If ICON(5) equal to 1
Bus voltage rectifier Freq_r = BSFREQ(Irect) * Freq_Nom_r
If ICON(5) equal to 2
Bus voltage inverter Freq_i = BSFREQ(Invrt) * Freq_Nom_i

2.3.2.2 **Converter Control**

The Converter Control provides the alpha_order as a function of the difference between current order and current response. For small signal analysis this may be enough. But for the large disturbances this basic function must be complemented by ,

Voltage Dependent Current Order Limiter

Current Control Amplifier, proportional part

Current Control Amplifier, integrator part

Linearization of Current Control Amplifier

Alphamax Calculation, AMAX

Alphamin Calculation, AMIN

Rectifier Alpha Min Limiter, RAML

Current Order Margin

Dalpha_limiter

A detailed description of the control function is found in the general description of the base control system, see ref.[2] and the PSS/E Application Guide, ref[5].

2.3.3 Internal Integration

The internal CCC equations are solved at each time step in the dynamic model. The values of overlap, alpha_prim and gamma_prim can not be directly solved why they are solved by iterations using Newton-Raphson methods.

To get results with acceptable precision and to avoid numerical instabilities the time step, DELT, must be selected smaller than the time constants of the HVDC control. Such a small time step is normally not acceptable in simulation of large systems.
An internal integration algorithm in the dc model has been introduced. The internal integration uses a simple relation as,

$$state(t+\Delta t) = state(t) + (\text{derivative at time } t) * \Delta t,$$

where Δt is the integration time step.
The internal integration is activated when the time step exceeds the constant, DELTMAX. Otherwise the integration of the HVDC model will be carried out by the normal PSS/E procedure.
The internal integration time step, is controlled by the parameter, DELTMAX,in the data file.

3 INTERFACE TO PSS/E

3.1 Load Flow HVDC Model

The data to be specified by the user are in accordance with the section referred to as "Two-Terminal DC Transmission Line Data" (see Section 4.1.1.7 in the PSS/E Program Operation Manual, Volume I).

The commutating capacitor reactance is specified in ohm per bridge. Entering a value which is greater than zero will represent a commutating capacitor. A value equal to zero will give a line commutated converter.

In a capacitor commutated converter the rectifier firing angles, (ALFMX and ALFMN) will represent the delay angle referring to the ac filter bus voltage. The inverter extinction angles (GAMX and GAMN) will specify the angles referring to the valve voltages.

3.2 Dynamic HVDC Model

The present d.c. model, CDCAB2, is actually written just for the dynamic part of PSS/E (pssds),

In fact what the present model does is to solve the d.c. system and afterwards update the data associated to the d.c. line specified in the power flow, during the dynamic simulation (see Section 6.4.7 "DC Transmission" on PSS/E Program Application Guide, Volume I).

The dynamic input data for the d.c. model is given in a file, while running activity "dyre", together with the definition of all other models used in the network.

The syntax is the following:

BUSID 'USRMDL' 0 'CBTBMD' IC IT NI NC NS NV Data_List/

where,

BUSID: d.c. line identity number

USRMDL: fixed name for user-written model

CBTBMD: name of the model

IC: equal to 7 (d.c. line model)[1]

IT: equal to 1 (current injection model)[1]

NI: equal to 10 (number of positions in ICON vector)[2]

NC: equal to 44 (number of positions in CON vector)[2]

NS: equal to 30 (number of positions in STATE vector)[2]

NV: equal to 100 (number of positions in VAR vector)[2]

Data_List: input data for the d.c. model itself

[1] Refer to PSS/E Manual.

[2] In PSS/E there are four large storage arrays named:

CON: contains constants;

STATE: contains state variables;

VAR: contains algebraic variables and

ICON: contains integer constants which may be either constants or algebraic integer variables

When using the model, the user should define how many positions the model is going to use in each of the big arrays mentioned before. In the present case (d.c. model) they are:

. 10 ICONs;

. 44 CONs;

. 30 STATEs and

. 100 VARs.

It has to be said that these figures are NOT supposed to be changed by the d.c. model user, since they are related to the model itself and not to the d.c. system that is being represented. This means that these figures are fixed values, independent of the system that is being studied.

After entering these data the user has to define the ICONs (10) and the CONs (44), since they actually represent the input data for the d.c. model.

The input is free-formatted and for the data identification, sequence and units one should follow the source code (available in Appendix) using the dynamic data file (dyn_proj.dyr) as a reference.

The input data can be verified by checking the printout from a validly specified load flow case and dynamic data in the dynamics working memory. The output is in the form of a Dynamic Data File and is activated by the selections, FILE, OUTPUT, Write dynamic data in source format (DYDA).

The dynamic data files described in the appendix see paragraph Data files, Dynamic Control Data.

3.3 Model Data

To make the model user friendly the parameter list of the data sheet has been limited to 44 constants. The remaining parameters (about 150) are specified in a separate data file (data_model.f). These parameters are internally stored in a common memory.
This data file is common for all the dynamic HVDC models in of type, CDCAB2, in the system. Contrary, all the constants specified in the dynamic data file (dyn_proj.dyr) can be set individually for each dc transmission.

The input data can be verified by reading the printout from the initiation stage. The activity DOCU produces a tabulated list of the model references in the dynamic setup. The storage locations used by the model in the various dynamic arrays are also listed

The selections, FILE, LIST, Dynamic Models and Data (DOCU) and Select bus number generate the parameter list.

The data list is described in appendix, see paragraph Data files, Dynamic Control Data.

4 USING THE HVDC MODEL

4.1 PSS/E Program Sections

Before using the d.c. model itself, the user should be aware of the PSS/E so called "activities", that are in fact the commands used to proceed in the simulations. In case of a new user, one should refer to Section 12 (Dynamic Simulation Setup) of PSS/E Program Application Guide, Volume II. There one can find an example of a small network setup and simulation procedures. Basically, a simulation comprises 3 major steps, as follow,

A.

Power flow calculation

PSS/E power flow calculation is started by typing ($ is the prompt):

$ psslf4

This module is mouse-driven and quite self-explanatory. An on-line HELP is also available.

B.

Dynamic simulation

This is started by typing:

$ pssds4

This module is mouse-driven and quite self-explanatory. An on-line HELP is also available.

C.

Output/plotting

It is invoked by typing:

$ pssplt

For detailed description see on-line HELP or PSS/E PSSPLT / IPLAN / TMLC binder.

4.2 PSS/E Operational Steps

To simplify the description, the procedures are divided into steps. A list of the files used and produced in that process is given below. See also the response files in the Appendix.

To get an organized structure of the files we have introduced the identity of the project in the file name as ,proj. The name of the response files starts with the name of the activity as solv, snap, strt ,run and so on.

Basic activity steps of a simulation:

Step 1: Get a power flow solution ($psslf4)

- Input file: flow_proj.raw

The input data can be checked by following Section 4 of PSS/E Program Operation Manual.

- Running: $psslf4

Data ® Input ® Read: lf_proj.raw

Powerflow ® Solution ® FNSL

Save as: proj.sav

Powerflow ® Reporting

Stop

Step 2: Compile the HVDC model

Compile the model file cfc_model.f

Compile the data file data_model.f

Where cfc_model.f : is the name of the dynamic HVDC model source code file.

Many attributes can be used for compiling (refer to the Fortran compiler manual for details) but the following two are essential for successful compilation:

-c:

only compilation is executed, suppressing the loading phase; notice that the model has to be linked later on to PSS/E.

-extend_source:

allows the statements in the source code to be extended up to 132 columns, instead of 72; the model was written using statements longer than 72 columns.

A more extended list of the attributes will be generated by the PSS/E program at the creation of the compile-file.

Step 3: Creating a snapshot and Routines Conet and Conec

Into file snap_proj.idv there are some activities that basically are responsible for creating a snapshot and form the files conet (.flx) and conec (.flx). The file snap_proj.idv is in fact a response file created by the activity echo (see activities echo and idev). For a good understanding of what is done by the activities into file snap_proj.idv, please refer to the example of Section 12 of the PSS/E Program Application Guide, Volume II. To run all the activities at once, one should invoke the file snap_proj(.idv) by applying activity idev:

Activity? idev snap_proj

- Files conec.flx (conec), conet.flx (conet) and proj.snp (snapshot) will be created on your working directory.

In the file snap_proj.idv there are two input files:

proj.sav:

it is the load flow saved case file.

dyn_proj.dyr:

it contains the dynamic input data for the models that will be used for the simulation. Looking into this file one can see that there are 3 dynamic models being used:

Twice GENCLS, that refer to the generators on the a.c. networks, and the d.c. model (CDCAB2). The associated data are the input data required by the models.

Step 4: Compiling routines Conet and Conec

For compiling these routines, one should run a file created by PSS/E, while creating the snapshot (step 3).

In this case, the file is called "compile" (see file snap_proj.idv), then, running it means:

$ compile

If it is the first time that the file "compile" is being used in an UNIX system, one should make it executable (on Dec-Alpha-OSF/1) by applying the command:

$ chmod + x compile (UNIX system only)

Step 5: Linking the model to PSS/E

The d.c. model object files (created by the compiler – f90) is linked to PSS/E by using the command below:

$ cload4 cfc_model.obj data_btb.obj (PC system)

$ cload4 cfc_model.o data_btb.o (UNIX system)

Step 6: Running the dynamics ($pssds)

As soon as step 5 is finished, PSS/E is ready to run a dynamic simulation, with the specified setup.

Here again, a response file is used for running the activities that are needed to start-up the dynamic simulation itself. The file is called strt_proj.idv. Basically what it does is to restore the snapshot that was created before (by using activity "rstr") and put the desired variables available for plotting and/or printing after the run. In PSS/E, the outputs are called "channels" and they are created by means of activity "chan".

After creating the channels, the system has to be started-up by using activity "strt" (see detailed description of activity "strt" on PSS/E manuals or on on-line help), and stating a name for the output file specified (this file will be used later on for plotting and/or printing when running pssplt).

Finished the start-up, the simulation is ready to begin. Similarly as before, the simulation is carried out interactively, by using PSS/E activities. It means that if the user wants to run a case up to time t_f and apply a disturbance at time t_d, the procedure to follow is:

- Run the case from time=-2*delt until time=t_d (use of activity "run");
- At time=t_d, apply the disturbance (use of activity "altr");
- Run the case from time=t_d until time=t_f (use of activity "run" again).

As mentioned before, the outputs of PSS/E runs are obtained by using the module called **pssplt**.

A set of some basic and useful activities for setting-up the plotting (only a reference to start with) are listed below:

$pssplt

Activity? **chnf** output_file

- chnf: select the channel output file

Activity? **rang**

- rang: allows the user to generate scales based on the current channel output file

Activity? **tint** t_i t_f

- tint: select time interval to plot

Activity? **popt**

- popt: allows the user to modify any of the program option settings currently in use

Activity? **slct**

- slct: select channels to be plotted; the channels are defined in activity "chan" (see file strt_proj.idv, Appendix III); the channels

numbers are defined sequentially as input in activity "chan"; to avoid counting, one can refer to activity "run", since a table with the channels and their associated numbers is created when running it.

Activity? **plot**

- plot: get the plotting

For more information about pssplt module, refer to PSS/E PSSPLT manual or to on-line help.

5 DATA FILES

5.1 Overview of data and response files

The files used to run a typical case are listed below:

Powerflow Files (psslf)

- flow_proj.raw Load Flow input data
- flow_proj.sav Load Flow solution
- solv_proj.idv Solve Load Flow, resp.file

Dynamic Data (pssds):

- dyn_proj.dyr Dynamic input data
- snap_proj.snp Snap shot file
- snap_proj.idv Generate snap shot,resp.file

HVDC Model Data (pssds):

- cfc_model.f HVDC model, source code
- cfc_model.obj (o) HVDC model, object code
- data_model.f Input data, source code
- data_model.obj (o) Input data, object code
- cfc_constants.ins Common area: /conline98/

Snapshots (pssds):

- snap_proj (.idv and .bin) Create a snap shot file

Start-up (pssds):

- strt_proj .idv Start up the dynamic simulation
- run_proj.idv Run the dynamic case

Output files (pssplt):

- out_proj .out	Output data
-plot_proj_step.idv	Plot Instruction
-plot_proj_acf..idv	Plot Instruction

5.2 Data structure

The files listed above, which are used to run the system, should be located in the working directory where the PSS/E program is activated..

5.3 Summary of commands

The PSS/E simulations can be activated by running the following sequence of response and command files:

psslf4

solv_proj

Stop

pssds4

snap_proj

Stop

compile

cload4

pssds4

strt_proj

run_proj

Stop

pssplt

plot_proj

Stop

6 SETTING UP THE DATA FOR THE HVDC MODEL

In the Appendix it is described in detailed how all the parameters are calculated and how to introduce the input data into the standard load flow model and dynamic data files.

The constants of the dynamic model can be set manually in the dynamic data file, dyn_proj.dyr, or if set equal to zero the corresponding values are picked up from the load flow solution.

7 MONITORING OF INTERNAL CALCULATIONS

The internal calculation of the HVDC model can be monitored at each calculation step by setting the appropriate plot-parameters. The parameter, Plot_on, activates the write/type instruction in the Fortran code and the text are stored in a separate file in the working directory.

The control parameter is included in the data file of the model.

The following types of print out is obtained,

Plot_on = 0

All output are disabled.

Plot_on = 1,2 or 3

Plot_on=1,A summary of internal calculation at each time step

Plot_on=2, Detailed calculation report.

Plot_on=3, All internal calculations are stored in a file.

This feature can be used to verify the internal calculations or during fault tracing of the HVDC model. During normal simulations all Plot Control switches should be set to zero otherwise the simulation time will be increased.

8 Operation of the transmission model

This section will give some instructions about how to handle the transmission model in different operation modes and which parameters should be checked. For each operation mode the corresponding input values should be checked. For instant, in current control mode the input data should be a current order and in power control the input data should represent a power order. Note that the name of the parameter is the same, 'Setval'.

Operation mode Current Control

Load Flow settings,

Mdc(idc)	2	Current control
Setval(idc)	3930	A

Dynamic Data settings,

Freq. and Damping Controllers deactivated

ICON(m+4)	0
ICON(m+5)	0

Operation mode Power Control

Load Flow settings,

Mdc(idc)	1	Power control
SetVal(idc)	1100	MW

Dynamic data settings

Freq. and Damping Controllers activated

ICON(m+4)	1 or 2
ICON(m+5)	1 or 2

Master Controller

Load Flow settings

Following load flow settings should be checked,

Mdc(idc)	1	Power controller activated
Vschd		kV
Vcmod		kV
ICON(m+1)		

Master Controller Settings

Active Power Controller

Following basic setting have been used as a default and defined in the data-file.

```
Ud_ref_mc = 0.0        ! Ref voltage pu, select hi or low time const
Ud_ref_min= 0.8        ! Min dc voltage, min limit in Udc_order
Tud_Mc_hi = 1.0        ! 1 sec
Tud_Mc_low = 0.1       ! 100 ms
```

Frequency Controller

Following basic setting have been used as default,

```
Kfc_prop = 1.0    !    Gain MW/Hz
Kfc_der = 1.0     !    Gain MW/Hz
Db_p    = 0.05    !    Dead Band prop
Db_d    = 0.05    !    Dead Band der.
Tfc_meas  = 0.1   !    Measuring filter
Tfc_der = 1.0     !    Der. filter
```

Damping Controller

Following basic setting have been usedas default,

```
Tdamp_1 = 0.1          Bandpass filter, high frequency, Tlow
```

Tdamp_2 = 1.0	Bandpass filter, low frequency, Thigh
Damp_Gain = -100.	Gain of the damping controller
Damp_Max = 50.	Max modulated power
Damp_Min = -50.	Min modulated power

AC NETWORK SYSTEM

Generator Model

GENCLS		Constant Internal Voltage Generator Model	
CONs	J	Inertia H	--> 1.0
	J+1	Damping constant D	--> 0.0

9 Verification test procedure

The stability of the transmission system should be investigated by checking the transient stability and the electromechanical stability.
The transient stability is checked by introducing current order step in the system and verify the current response.
The electromechanical stability of the transmission system is verified by adjusting the parameters of the control system to damp out oscillations in the system while monitoring the transient stability of the HVDC system. In the test setup, the machine can be simulated without damping and the HVDC is used to damp out the oscillation started after a disturbance in the system.

This verification tests are recommended to be performed in the following sequence.

Step 1.

Check the actual parameter settings. See data in this report
- Data sheet
- Data file parameters
- Converter data

Step 2.

Create and prepare working directories.
Transfer required files to the working directories
Set up the transmission system.
Run steady state to verify all files.

Step 3.

Run the complete transmission system
Check stability by making a current order step
Simulate a fault.
Activate the damping controller
Adjust control parameters to stabilize the system.

10 REFERENCES

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The concept of capacitor commutated converter stations.
1JNL100010-874

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Control Principles. 1JNL100004-959

[3] CIGR 1996:14-102
New Concepts in HVDC Converter Station Design

[4] Main circuit calculation program
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[5] PSS/E Program Application Guide
Model CDCAB1,
ABB Detailed DC line model, CDCAB1

[6] PSS/E Program Operation Manual
III.4.3 Non-Standard Models,
ABB DC line model, CDCAB1

[7] Brazil – Argentina Interconnection
Main circuit design and reactive power characteristics
1JNL100022-050

11 APPENDIX BACK-to-BACK MODEL

This DC transmission presents a typical example with a Back-to-Back transmission designed with CCC converters. At nominal operation conditions this dc transmission operates with negative delay angle in rectifier and the inverter is used to generate reactive power into the ac network. The short circuit ratio of the inverter is very low why the amplitude of ac voltages is very sensitive to changes in reactive power.

11.1 Argentina–Brazil Electrical Interconnection at Garabi

Basic HVDC Data of the transmission

This appendix presents the procedure to set up an HVDC transmission and how to determine the input data and how to run it. When this basic system is running correct the simple ac networks can be replaced with more detailed networks.

The appendix presents the calculations of the basic design data of an HVDC/CCC Back-to-Back transmission system and describes the procedure how to setup the standard load flow model and also how to run the dynamic non standard user model, CDCAB2.

The HVDC Back-to-Back dc transmission is set up to obtain a test case where the HVDC/CCC model can be tested in a simple network. Each ac system is represented by an infinite source with external short circuit impedance and a short ac transmission line on the receiving side.

The technical solutions for the proposed back-to-back station are chosen to present the basic back-to-back transmission system. The proposed solution is a modular back-to-back design according to the ABB HVDC/CCC concept.

The presented test cases are designed for a power transmission of 1100 MW between two ac system and is set up both in a single block and in a double block configurations. Each block is defined as one rectifier and one inverter 12-pulse converter connected in a back-to-back configuration.

The ac transmission is set up according to the main circuit report of the Argentina-Brazil Electrical Interconnection at Garabi, see ref[7]. Each ac system is represented by an infinite source with a short circuit impedance and an ac transmission line on the Brazilian side.

The system has been setup in both PSS/E and EMTDC. The result of the verification study is presented in a separate ABB report. The following paragraph presents the procedure to calculate the model data of the HVDC transmission.

In the PSS/E program, the load flow dc transmission is built up by a number of series connected 6-pulse converters, 4x275 MW.
The HVDC back-to-back converter station is connecting the 50 Hz network of Argentina with the 60 Hz network of Brazil. The converter station shall be capable of a power transmission corresponding to 1000 MW delivered to the substation at

Ita´ in Brazil or Rincon St. Maria in Argentina. The site is located near Garabi, in Brazil not far from the border to Argentina. A 525 kV a.c. line from the back-to-back station to the Ita´ station in Brazil, and a 500 kV a.c. line to the Rincon St. Maria station in Argentina will be built.

The presented examples are setup for a power transmission of 1100 MW from Argentina to Brazil and show both a single block and a double block configurations.
The ac networks have been reduced to simple impedance connected to infinite sources.

The dynamic HVDC Non Standard User Model, CDCAB2, presented in this memo, HVDC control model is specified by applying data in the following documents,

Data sheet	CDCAB2	HVDC Transmission Model
Model file	cfc_model_926.f	Fortran file
Data file	data_btb_926.f	Fortran file

Common settings for the HVDC control
(These parameters are available and can be changed by the advanced users)
Declaration file cfc_constants_926.ins

The model version '926' is referring to year 1999 and week 26 and also referring to version 26 of PSS/E.

The main circuit calculation is performed by using the ABB application program, "Main circuit calculation program for conventional and Capacitor Commutated Converters"

12.1.2 PSS/E DC Transmission Model

Background: PSS/E program is composed basically of three packages: Power Flow, Dynamics and Plotting.
The goal is to get reasonable initial settings of the power flow that corresponds to a case, which can be solved. If the initial data is not correct a solution may not be found, and the system blows up, reflecting a bad initialization.

The ABB Main Circuit Calculation Program is used to design the CCC converter to be included in the load flow model. If the dc transmission is already designed the actual main circuit data can be used and the calculation is not required.

The setup of the HVDC dynamic transmission model in the PSS/E program has been updated to load flow model of version 26.2 of the PSS/E program and the solved parameters from the load flow is used as initial conditions of the dynamic simulation.

The dynamic model is non standard user model in PSS/E, called CDCAB2. This model represents one two terminal dc transmission with the following features,

- Line/Cable model
- Back-to-Back model
- Conventional line commutated converter, LCC
- Capacitor commutated converter, CCC
- Mixed types of converters both CCC and LCC

The dynamic model has been used internally at ABB Power Systems.

11.2 Calculation of AC System parameters:

The calculated values used in the load flow model is indicated by bold digits.

11.2.1 Rectifier Side:

System Base: 100 MVA
Base Voltage = 500 kV
Base impedance = 2500 Ohm
Base suceptance = 1 / 2500 = 0.0004 mho = 400 umho

Infinite AC bus voltage: 1 pu , 0 degree

Zsc = 0.0147 pu -> 36.75 ohm -> Ssc= 6944 MVA

50 Hz, -> w = 314.159

Rectifier Side: AC Filter

B_1 = 170 + 9.15 = 179.15 MVar for 1 pu voltage
(ac - filter + PLC-filter)

Rectifier Side: AC Reactor

Br_1 = **92.5** MVAr for 1 pu voltage

11.2.2 Inverter Side

Base Voltage AC bus voltage: 1 pu = 525 kV
Ibase = 100 / 525 = 0.1905 kA
Zbase = (525*525) / 100 = 2756.25 Ohm
Suseptanse_base = 362.8 umho

60 Hz, -> w = 376.99
Source impedance
Zsc = 0.0147 pu -> 40.05 ohm -> 6882 MVA

AC Transmission Line

AC Line data:
4 Rook Conventional design l = 360 km

---> R = 8.49 Ohm,
X = 114.85 L = 304.65 mH
B = 1805 umho ->

Ctotal = 4.78 uF = 2*2.39 uF
--> 1805 / 362.8 = 4.975 pu

B/2 = 2.488 pu

R = 8.49	Ohm-	-->	**0.00308**	pu
X =114.85	Ohm	-->	**0.04167**	pu

B = 497.5 MVAr for 1 pu voltage -> B/2 = 248.8 MVAr

Inverter Side: AC Filter
Harm.filter+PLC filter
B_2 = 2*85+22.1= 192.1 MVAr for 1 pu voltage

Total MVAr at inverter bus
B_2 + B/2 = 192.1 + 248.8 = 440.9 MVAr

Inverter Side: AC Reactor

Br_2 = **250** MVAr fixed shunt

Ita' shunt reactor

Br_2 = **150** MVAr

DC Side

Smoothing reactor	100 mH/550 MW block or 200 mH/1100 MW block
Resistor	0.4 Ohm/550 MW block or 0.8 Ohm/1100 MW block

DC Converter

DC Power	550 MW/block
DC Voltage	140 kV/12-pulse
DC Current	3930 A

Converter Transformer

Rectifier

Ac voltage		500 kV
Valve voltage	Uv = 51.5	kV
Transformer ratio		ttr=UvN/UtN = 51.5/500 = **0.1030**

Inverter

Ac voltage		525 kV
Valve voltage	Uv = 51.5	kV
Transformer ratio		ttr=UvN/UtN = 51.5/525 = **0.0981**

11.2.3 PSS/E Load Flow Converter Design

The values to be included in the raw data file are indicated by bold figures.

Calculation of equivalent load flow model.
Nominal value Rectifier

Udio = 3 / pi * Sqr2 * 51.8 = 69.95 kV/ 6p-group
dxl = 0.06
Uv=52.4085 kV
L = 3.55878 mH
XCR = 2*pi*50*3.56234*E-3=**1.118 Ohm**

dxc = 0.20
Qc=31.59 MVAr/phase
Ucpeak=15.35 kV
C=853.3 uF
XCAPR= 1 / (2*pi*Freq*C) = **3.7303** ohm

Qdc = 0.05218 pu UdcN = 57.3 MVAr

Alpha = **-5.7** deg,
Alpha_prim = 14.06
Overlap = 12.69 deg

Nominal value, Inverter

Udio = 3 / pi * Sqr2 * 51.5038 = kV/ 6p-group
dxl = 0.072
Uv=51.5038 kV
L = 3.62332 mH
XCI = 2*pi*50*3.62332*E-3=**1.366** Ohm

dxc = 0.34
Qc=-53.7 MVAr/phase
Ucpeak=26.10 kV
C=418.3 uF
Freq. = 60 Hz
XCAPI= 1 / (2*pi*Freq*C) = **6.3418** Ohm

Qdc = -0.0729 pu PdcN ->-76.5Mvar

Overlap = 13.57 deg

Inverter(Gamma 21.7 deg)
Freq = 60 Hz
Alpha = 177.69 deg,
Gamma_prim = **21.7** deg
Overlap = 13.57 deg

Reference Matlab-files See calculated result below in next paragraph.

Reference: C:\matlab\mfile\garabi\pti_26.2\btb1100_r.m
C:\matlab\mfile\garabi\ pti_26.2\btb1100_i.m

11.2.4 Garabi Control parameters,

A base design control system has been used with standard settings. Following parameters have been updated according to an EMTDC study of the Garabi.

Control Amplifier

CCA Gain Rect		80	deg/pu.IdN
Ti		0.5	ms
CCA Gain Inv		40	deg/pu.IdN
Ti		0.4	ms
Gamma_ref		21.7	deg
Io_Margin		0.03	pu
Alpha Max Lim 178 ->		200	deg
Alpha Min	-	9.8 ->	14 deg

Rectifier Alpha Min Limiter

Activated at Udc-level	ultrpu = 0.50	pu
Dealy angle increased	datr = 40.0	deg
Dealy angle increased	dbtr = 40.0	deg
Delay on	t1tr = 0.02	sec
Dela y off	t2tr = 0.01	sec
Delay off step	t3tr = 0.01	sec
Ramp time	t4tr = 0.125	sec

Ref: File: data_model_btb.f

11.2.5 Load Flow Solution Calculation

The constraints for the capacitor commutated converters are a system of linear equations. When both rectifier and inverter are capacitor commutated each converter's system of equations may be coupled or decoupled to the other depending on the control mode. The converter state must be obtained by solving these converter equations simultaneously. A Newton-Raphson solution process is employed for the capacitor commutated dc line. This process is iterative and depending on the condition of the problem it may fail to converge and thus may fail to provide the ac solution process with reliable dc boundary condition for each iteration. Newton solution control parameters, including iteration limit and acceleration factor are provided with the two-terminal dc line data.

The user of the CCC model should watch the calculation reports and should be careful not to accept a faulty solution where the convergence criteria has not been fulfilled.

The number of iteration may be increased from 20 to 200 by the selection,

EDIT, Load Flow Data, Solution Parameters, Newton Solution Parameters

It may also be advantage to start the iteration with a fixed slope or decoupled solution method before the Full Newton-Raphson method is used.

Before going to dynamic simulations the loads must be converted by the activities CONL and CONR.

The generators are converted by the activity CONG.

The actual dc values can be presented by the command,

Interrupt (F10), Power Flow, Solution, FNSL, Select interrupt code ‘DC’.

11.2.6 Dynamic Simulation

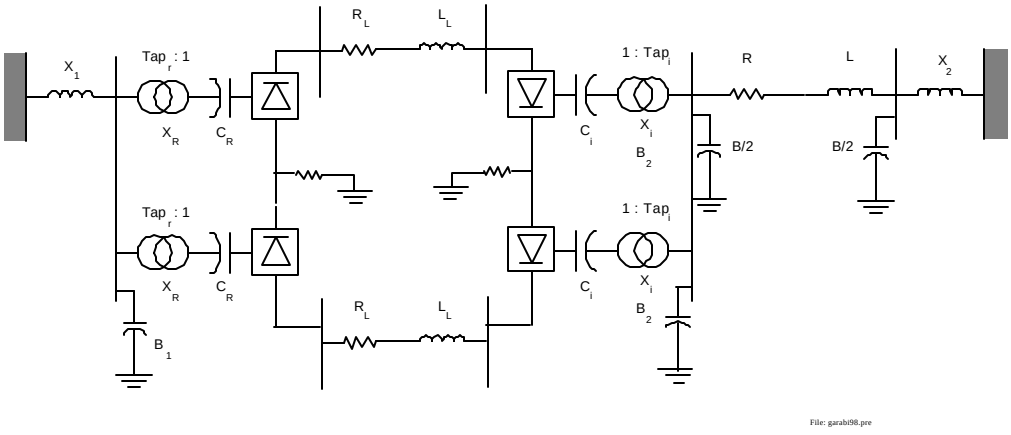
It is recommended to select a very small time step to get correct representation of the fast transients of the dc transmission. For a good result a time step of 0.1 ms should be selected.
If the fast transients are not important for the study result, the time step can be increased but the time step should be less to about 5 ms to avoid unstability.

The actual back-to-back transmission is grounded in the middle with one 6-pulse group connected to each pole.

11.2.7 Dynamic Model Configuration

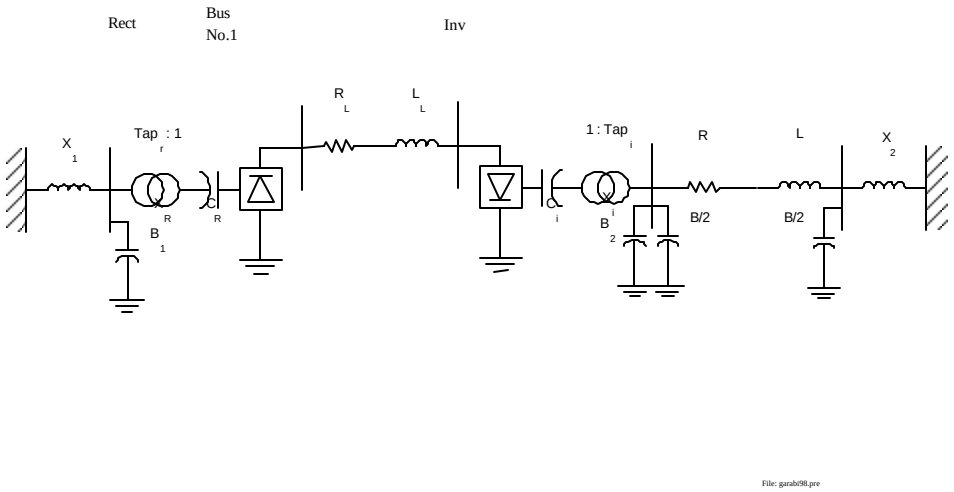
HVDC/CCC TRANSMISSION CONCEPT

Back to Back Converter Block



The actual back-to-back transmission is grounded in the middle with one 6-pulse group connected to each pole.

PSS/E DYNAMIC MODEL



The HVDC transmission is modeled as a monopolar transmission link with serie connected 6-pulse groups.

12 Single Block Model

PSS/E SETUP, Basic 4x270 MW:

CCC_Development. Reduced ac network

Reference cases,

Block/Deblock	Manual Block/Deblock	Power reduction 1100 MW
Run	power transmission	0, 0.1, 0.2, 1.0 pu Pdc
Step in current order	+10%	run_btb300_step.idv

12.1 Load Flow Setup of ac system

AC System:

12.1.1 Rectifier Side:

System Base: 100 MVA
Base Voltage = 500 kV
Base impedance = 2500 Ohm
Base suseptance = 1 / 2500 = 0.0004 mho = 400 umho

12.1.2 Inverter Side

Infinite AC bus voltage: 1 pu = 525 kV
Ibase = 100 / 525 = 0.1905 kA
Zbase = (525*525) / 100 = 2756.25 Ohm
Suseptanse_base = 362.8 umho

Ssc = 6800 MW
Zsc = 525*525 / 6800 = 40.5 Ohm
Zsc = 40.5 --> 0.0147 pu

AC Transmission Line
R = 8.49 Ohm- -->0.00308 pu
X =114.85 Ohm --> 0.04167 pu

B = 497.5 MVAr for 1 pu voltage -> B/2 = 248.8 MVAr

Short circuit capacity at Garabi
Ssc=1 / (0.0147+0.04167) pu => 1774 MW

Inverter Side: AC Filter
Harm.filter+PLC filter
B_2 = 2*85+22.1 = 192.1 Mvar for 1 pu voltage

B_2 + B/2 = 192.1 + 248.8 = 440.9 MVAr

Inverter Side: AC Reactor

Br_2 = 250 MVAr fixed shunt

Ita shunt reactor

Br_2 = 150 MVAr

DC Side

Single block transmission, 1100 MW

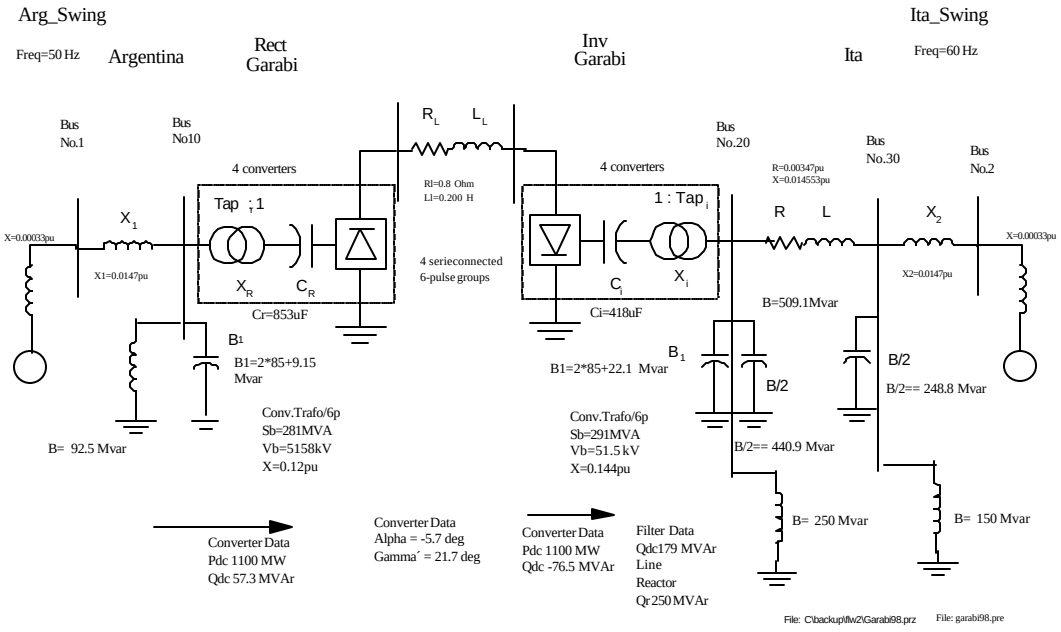
Smoothing reactor	200 mH/1100 MW block
Resistor	0.8 Ohm/1100 MW block

Double block transmission, 2x550 MW

Smoothing reactor	100 mH/1100 MW block
Resistor	0.4 Ohm/1100 MW block

PSS/E GARABI - ITA HVDC TRANSMISSION

Argentina - Garabi PSS/E Study



12.2 Load Flow Data File

```
0,   100.00          / THU, JUL 08 1999  11:10
<GARABI SYSTEM: CCCGARABI1/FLOW_BTB.RAW>
<1100 MW POWER TRANSFER, REDUCED NETWORK>
    1,'ARG_SW  ', 500.0000,3,     0.000,     0.000,   1,   1,1.01000,
0.1000,   1
    2,'ITA_SW  ', 525.0000,3,     0.000,     0.000,   1,   1,1.00500,
0.2000,   1
   10,'GARABI_A', 500.0000,1,     0.000,     0.000,   1,   1,0.99993,  -
9.1167,   1
   20,'GARABI_B', 525.0000,1,     0.000,     0.000,   1,   1,1.00260,
36.6982,   1
   30,'ITA     ', 525.0000,1,     0.000,     0.000,   1,   1,0.96625,
9.3421,   1
0  / END OF BUS DATA, BEGIN LOAD DATA
   10,'1 ',1,   1,   1,     0.000,    92.500,     0.000,     0.000,
0.000,     0.000,   1
   20,'1 ',1,   1,   1,     0.000,   250.000,     0.000,     0.000,
0.000,     0.000,   1
   30,'1 ',1,   1,   1,     0.000,   150.000,     0.000,     0.000,
0.000,     0.000,   1
0 / END OF LOAD DATA, BEGIN GENERATOR DATA
    1,'1 ',  1100.400,   157.887,  9999.000, -9999.000,1.01000,    0,
1000.000,   0.00330,   0.00333,   0.00000,   0.00000,1.00000,1,  100.0,
9999.000, -9999.000,   1,1.0000
    2,'1 ', -1049.586,   348.850,  9999.000, -9999.000,1.00500,    0,
1000.000,   0.00330,   0.00333,   0.00000,   0.00000,1.00000,1,  100.0,
9999.000, -9999.000,   1,1.0000
0 / END OF GENERATOR DATA, BEGIN BRANCH DATA
    1,    10,'1 ',   0.00000,   0.01470,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
    2,   -30,'1 ',   0.00000,   0.01470,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
   20,    30,'1 ',   0.00308,   0.04167,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
0 / END OF BRANCH DATA, BEGIN TRANSFORMER ADJUSTMENT DATA
0 / END OF TRANSFORMER ADJUSTMENT DATA, BEGIN AREA DATA
0 / END OF AREA DATA, BEGIN TWO-TERMINAL DC DATA
  1,2,    0.8000,   3930.00,    280.00,      0.00,    0.8000,   0.10000,'R',
0.00,  20,   1.00000
   10, 4,-5.70,-5.70, 0.0001, 1.1180,
500.0,0.1030,0.99495,1.11000,0.98000,0.00000,    0,    0,    0,'1 ', 3.7305
   20, 4,21.70,21.70, 0.0001, 1.3660,
525.0,0.0981,1.00857,1.11000,0.90000,0.00000,    0,    0,    0,'1 ', 6.3418
0 / END OF TWO-TERMINAL DC DATA, BEGIN SWITCHED SHUNT DATA
   10,0,1.00000,1.00000,    0,  170.00, 1, 170.00
   20,0,1.00000,1.00000,    0,  441.00, 1, 441.00
   30,0,1.00000,1.00000,    0,  249.00, 1, 249.00
0 / END OF SWITCHED SHUNT DATA, BEGIN IMPEDANCE CORRECTION DATA
0 / END OF IMPEDANCE CORRECTION DATA, BEGIN MULTI-TERMINAL DC DATA
0 / END OF MULTI-TERMINAL DC DATA, BEGIN MULTI-SECTION LINE DATA
0 / END OF MULTI-SECTION LINE DATA, BEGIN ZONE DATA
0 / END OF ZONE DATA, BEGIN INTER-AREA TRANSFER DATA
0 / END OF INTER-AREA TRANSFER DATA, BEGIN OWNER DATA
0 / END OF OWNER DATA, BEGIN FACTS CONTROL DEVICE DATA
0 / END OF FACTS CONTROL DEVICE DATA
```

12.3 Dynamic Model Setup

12.3.1 Dynamic Model

The dynamic HVDC model includes following features

HVDC Model used in conec	CDCAB2	cfc_model_926.f
HVDC Model used in conet	TDCAB2	cfc_model_926.f
Data sheet	see next paragraph	
Data file	data_btb_926.f	
Declaration file	cfc_constants_926.ins	

The input data is described in the Data Sheet of the model, see paragraph 15.

12.3.2 Dynamic Model Data File

Example of the dynamic data listing,

```
 1, 'GENCLS', 1, 0.0, 0.0 /  Update 990701
 2, 'GENCLS', 1, 0.0, 0.0 /
 1  'USRMDL'  0 'CDCAB2' 7 1
                     10 44 30 100
                     1 0 0 0 0 0 0 0 3 2
                     4.02
                     280.0  3.930
                     50.00  0  60.0  0  0  0
                     0 0 0 0 0 0 0 0
                     200
                     0 0 0 0 0 0
                     0.005 0.06  0.8 0.2 0.1 2.0 0.3
                     0.005 0.055 0.8 0.2 0.1 2.0 0.3
                      80.0 0.0005 40.0 0.0004
                      0 0/
/
```

Example of the DYDA list of parameters.

```
DYNAMIC DATA OF DC-LINE :           1
     ----   C O N S T A N T S  ----
 ICON(           0)=           1
 ICON(           1)=           0
 ICON(           2)=           0
 ICON(           3)=           0
 ICON(           4)=           0
 ICON(           5)=           0
 ICON(           6)=           0
 ICON(           7)=           0
 ICON(           8)=           3
 ICON(           9)=           2
 CON(           0)=   4.020000         CON(           1)=   280.0000
 CON(           2)=   3.930000         CON(           3)=   60.00000
 CON(           4)=   1.000000         CON(           5)=   60.00000
 CON(           6)=   1.000000         CON(           7)=  0.0000000E+00
 CON(           8)=  0.0000000E+00     CON(           9)=  0.0000000E+00
 CON(          10)=  0.0000000E+00     CON(          11)=  0.0000000E+00
 CON(          12)=  0.0000000E+00     CON(          13)=  0.0000000E+00
 CON(          14)=  0.0000000E+00     CON(          15)=  0.0000000E+00
 CON(          16)=  0.0000000E+00     CON(          17)=   200.0000
 CON(          18)=  0.0000000E+00     CON(          19)=  0.0000000E+00
 CON(          20)=  0.0000000E+00     CON(          21)=  0.0000000E+00
 CON(          22)=  0.0000000E+00     CON(          23)=  0.0000000E+00
 CON(          24)=  4.9999999E-03     CON(          25)=  5.9999999E-02
 CON(          26)=  0.8000000         CON(          27)=  0.2000000
 CON(          28)=  0.1000000         CON(          29)=   2.000000
 CON(          30)=  0.3000000         CON(          31)=  4.9999999E-03
```

```
CON(          32)=  5.5000000E-02     CON(          33)=  0.8000000
CON(          34)=  0.2000000         CON(          35)=  0.1000000
CON(          36)=   2.000000         CON(          37)=  0.3000000
CON(          38)=   80.00000         CON(          39)=  5.0000002E-04
CON(          40)=   40.00000         CON(          41)=  3.9999999E-04
CON(          42)=  0.0000000E+00     CON(          43)=  0.0000000E+00
```

12.3.3 Model Data

Example of the DOCU listing of parameters.

```
DC-LINE    IDC,       M,       J,       K,         L:
         1        1        5        5        1
    ----  C O N  ----
 ************************************
  -----  ICONs  -----:
 Transmission System Parameters:
 System Type: Back-to-Back Transmission
 Converter Type: Rectifier and Inverter CCC
 Current direction:          1   Rect=1 Inv=0
 Freq.Control:               0   Rect=1  Inv=2
 Damp.Control:               0   Rect=1 Inv=2 Ext=3
  -----  CONs  -----:
 Frequency Controller:
 Frequency Control disabled:
 Kfc_prop:       1.000000     Gain MW/H
 Kfc_der:        1.000000     Gain MW/H
 Db_p:       5.0000001E-02Dead Band prop
 Db_d:       5.0000001E-02Dead Band deriv.
 Tfc_meas:      0.1000000    Measuring filter
 Tfc_der:       1.000000    Der filter
 --- Damping Controller  ------:
 Damping Control disabled:
 Tdamp_1:       0.1000000
 Tdamp_2:       1.000000
 Damp_Gain:      -100.0000
 Damp_Max:       50.00000     Max limit
 Damp_Min:      -50.00000     Min limit
 ---  Master Controller  ------:
 Current Control active:
 Current Order =     3930.000     A
 Ud_ref_mc:       0.8000000    Ref voltage pu
 Ud_ref_min:      0.8000000    Min voltage pu
 Tud_Mc_hi:       1.000000
 Tud_Mc_low:      0.1000000
 IOMAX_MASTER:       4.020000
  --- HVDC System Paramerer:
 UdN:       280.0000
 IdN:       3.930000
 Freq_Nom_r:       50.00000
 CCC_ind_r:       1.000000
 Freq_Nom_i:       60.00000
 CCC_ind_i       1.000000
  --- Converter dx & dr:
…..
```

and so on

12.3.4 Response Files

solv_lf.idv	Solving the Load Flow model
snap_btb.idv	Snap shot saved in file btb.sav
strt_btb.idv	Start of simulated case with time step 0.1 ms
run_btb_step.idv	Run 300 ms with a 10 % Current order step
plot_btb_step.idv	Plotting the result of the control variables, 300 ms

12.3.4.1 Solve Load Flow

Manually command steps,

RAED, ALL, Raw data file

CHNG, change the iteration steps 20 -> 200

FDNS, OPT, run decoupled Newton Raphson

FNSL,OPT run full Newton Raphson

BAT_CONL, converge loads

CONG, converge generators

SAVE the case in file flow_btb

Response file:

```
MENU,OFF      /* ver.26.2.2
READ,ALL
flow_btb.raw
CHNG
7
Y
,,,,
Y
0.6,,200
Y
,,
Y
,,,,,
0             / TO EXIT CHNG
FDNS,OPT
0,0,0,0,0,0
99
FNSL,OPT
0,0,0,0,0,0
99
BAT_POUT 0 1
BAT_CONL 0 1 1 0 0     80.00     20.00     50.00     50.00
BAT_CONL 0 1 2 0 0     80.00     20.00     50.00     50.00
BAT_CONL 0 1 3 0 0     80.00     20.00     50.00     50.00
CONG
BAT_RAWD 0 1 1 1 1 1 0 0
"flow_btb"
SAVE
flow_btb
ECHO
@END
```

12.3.4.2 Creat a Snap Shot

```
MENU,OFF /* ver.26.2.2, output snap_btb.idv
LOFL
CASE
flow_btb.sav
ORDR
FACT
RTRN
DYRE
dyn_btb.dyr
conec.flx
conet.flx

,,,
compile
SNAP
snap_btb.snp
,,,,
ECHO
@END
```

12.3.4.3 Start of dynamic simulation

```
MENU,OFF  /* 990708 Status, ver.26.2.2,strt_*.idv
RSTR
snap_btb.snp
LOFL
CASE
flow_btb.sav
CONG
FACT
RTRN
DOCU,ALL
2
docu_btb.dat
0
CHAN
1,101,11
13
10,'ret-ac_volt'
20,'inv-ac_volt'

20
5,'Idc_r-<kA>'
8,'Idc_i-<kA>'

19
1,'Pac_r>pu>'
2,'Qac_r<pu>'
3  'Pac_i <pu>'
```

```
4  'Qac_i <pu>'
6  'Iorder_r<pu>'
7  'Iorder_i<pu>'
8  'i_error_r<pu>'
9  'aprop_r<pu>'
10 'alfa_order_r'
11 'amin_cca_r'
13 'i_error_i<pu>'
14 'aprop_i'
15 'alfa_order_i'
16 'amin_cca_i'
17 'amax_cca_i'
18 'alfa_cfc_r'
19 'alfa_cfc_i'

14
1  'Volt-R-1'
   'Ang-R-1'
2  'Volt-R-2'
   'Ang-R-2'

13
10,'ret-ac_volt'
20,'inv-ac_volt'

0
ALTR
6
N
Y
,,0.0001,,,
N
N
0
0
STRT
start.out
0
ECHO
@END
```

12.3.4.4 Run a 10% step in current order

```
MENU,OFF      /* FORCE MENU TO CORRECT STATUS
RUN
0.05000,10,10,0
ALTR
0
1
0
```

```
6
1
N
Y
,3537.0,,,,,,,,
-1
0              / TO GET TO CATEGORY SELECTOR
0
RUN
0.1500,10,10,0
ALTR
0
1
0
6
1
N
Y
,3930.0,,,,,,,,
-1
0              / TO GET TO CATEGORY SELECTOR
0
RUN
0.300,10,10,0
ECHO
@END
```

12.3.4.5 Plot a 10% step in current order

```
MENU,OFF      /* FORCE MENU TO CORRECT STATUS
CHNF
M:\PSSE26\CCCgar926_06\start.out
RANG
1

TINT
0.000000 0.300000

SLECT PLOT SIGNALS
…..
….
CLSP


SLCT
9
R
28
R
9
0.7000 1.2000
28
```

```
0.2000 1.2000
0
PLOT,IN
26
Step +10%
41
SLCT
9
R
28
R
9
0.7000 1.2000
28
0.2000 1.2000
0
PLOT,IN
Step +10%
41
SLCT
26
R
27
R
28
R
26
0.9000 1.1500
27
0.9000 1.15000
28
0.7000 1.2000
0
PLOT,IN
Step +10%
41
41
CLSP
1,\\POWNT_S\K1PS15
STOP
```

12.3.5 BAT Files

The PSS/E program requires a sequence of actions to perform the compiling and linking tasks.

Following bat-files are used to simplify the actions,

compile.bat,	compiling conec.flx and conet.flx
comp_926.bat	compiling cfc_model_926.f and data_btb_926.f
link_926.bat	linking conec, conet cfc_model _926 and data_btb_926

compile.bat (generated by the PSS/E program)

```
          @ECHO OFF
FLECS32 conec.flx -L NO -F PSS001.FOR -EXPAND -W 100 -S * "C:\PSSE25W\PSSLIB" -F77
DF /4L132 /4Ya /4Nd /nologo /fpscomp:logicals /c /4Nportlib /Fo"CONEC.OBJ" /D"DLLI" /MD
PSS001.FOR /I"C:\PSSE25W\PSSLIB"
DEL PSS001.FOR
          @ECHO OFF
FLECS32 conet.flx -L NO -F PSS001.FOR -EXPAND -W 100 -S * "C:\PSSE25W\PSSLIB" -F77
DF /4L132 /4Ya /4Nd /nologo /fpscomp:logicals /c /4Nportlib /Fo"CONET.OBJ" /D"DLLI" /MD
PSS001.FOR /I"C:\PSSE25W\PSSLIB"
          DEL PSS001.FOR
          REM
          ECHO If no errors, execute "CLOAD4"
```

PC version

Comp_926.bat (written manually derived from compile.bat)

```
@ECHO OFF
REM FLECS32 hvdcl.flx -L NO -F PSS002.FOR -EXPAND -W 100 -S * "C:\Program
Files\PTI\PSSE26\PSSLIB" -F77

DF /4L132 /4Ya /4Nd /nologo /fltconsistency /fpscomp:logicals /c /4Nportlib
/Fo"cfc_model_926.obj" /D"DLLI" /MD cfc_model_926.f /I"C:\Program
Files\PTI\PSSE26\PSSLIB"
DEL PSS002.FOR
REM
ECHO *** CFC MODEL FILE COMPILED ***

REM FLECS32 hvdcl.flx -L NO -F PSS002.FOR -EXPAND -W 100 -S * "C:\Program
Files\PTI\PSSE26\PSSLIB" -F77

DF /4L132 /4Ya /4Nd /nologo /fltconsistency /fpscomp:logicals /c /4Nportlib
/Fo"data_btb_926.obj" /D"DLLI" /MD data_btb_926.f /I"C:\Program
Files\PTI\PSSE26\PSSLIB"
DEL PSS002.FOR
ECHO *** DATA FILE COMPILED ***
ECHO If no errors, execute "HVDCL-CLOAD4"
```

PC version

Link_926.bat (written manually)

```
cload4 cfc_btb18.obj data_btb18.obj
ECHO  *** LINK COMPLETE ***
```

13 Double Block Model

PSCAD/EMTDC SETUP 2x550 MW CONVERTER BLOCKS

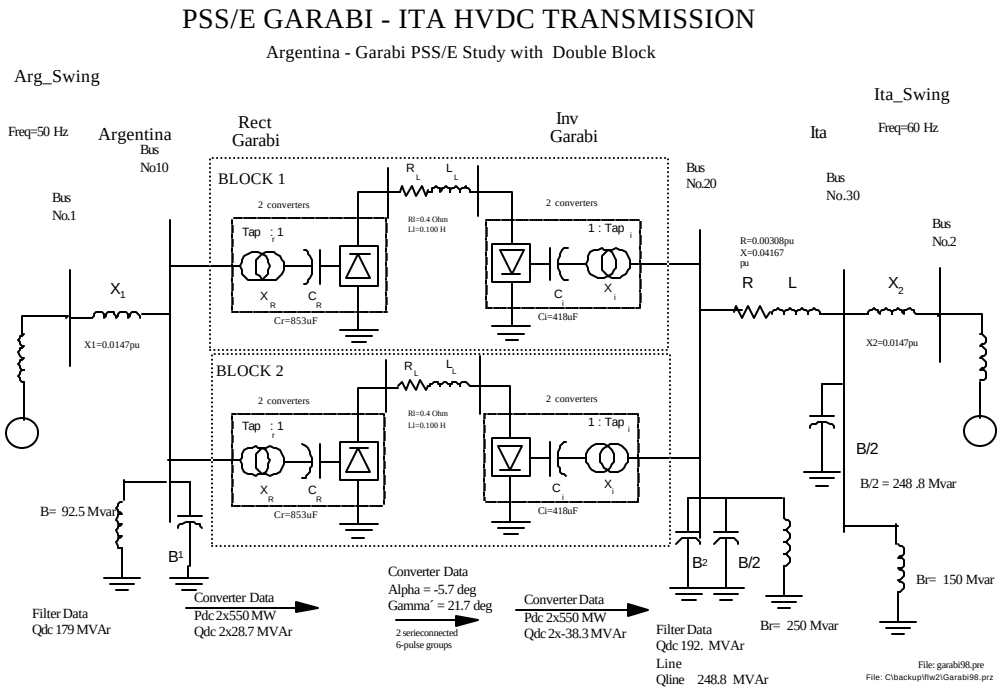
Reference cases,

Block/Deblock	Manual Block/Deblock Power reduction 550 MW	
Step in current order	-10% at 0.2 sec parallel operation of two block +10% at 0.5 sec	
Response file	run 1 sec	run_btb_step.idv
	plot plot_btb_step.idv	
	plot file	step.bin

13.1 Load Flow Setup

The ac system is setup in the same way as in paragraph 13.2.1.

The HVDC converter is split into two different block of 550 MW in each block.



13.2 Load Flow Data File

```
0,   100.00          / THU, JUL 08 1999  15:43
<GARABI SYSTEM: CCCGARABI1/FLOW_BTB.RAW>
<1100 MW POWER TRANSFER, REDUCED NETWORK>
    1,'ARG_SW  ', 500.0000,2,     0.000,     0.000,   1,   1,1.01000,
0.1000,   1
    2,'ITA_SW  ', 525.0000,2,     0.000,     0.000,   1,   1,1.00500,
0.2000,   1
   10,'GARABI_A', 500.0000,1,     0.000,     0.000,   1,   1,0.99993,  -
9.1167,   1
   20,'GARABI_B', 525.0000,1,     0.000,     0.000,   1,   1,1.00260,
36.6982,   1
   30,'ITA     ', 525.0000,1,     0.000,     0.000,   1,   1,0.96625,
9.3421,   1
0  / END OF BUS DATA, BEGIN LOAD DATA
   10,'1 ',1,   1,   1,     0.000,     0.000,     0.000,    46.253,
0.000,   -46.257,   1
   20,'1 ',1,   1,   1,     0.000,     0.000,     0.000,   124.676,
0.000,  -124.353,   1
   30,'1 ',1,   1,   1,     0.000,     0.000,     0.000,    77.620,
0.000,   -80.331,   1
0 / END OF LOAD DATA, BEGIN GENERATOR DATA
    1,'1 ',  1100.400,   157.887,  9999.000, -9999.000,1.01000,    0,
1000.000,   0.00330,   0.00333,   0.00000,   0.00000,1.00000,1,  100.0,
9999.000, -9999.000,   1,1.0000
    2,'1 ', -1049.586,   348.850,  9999.000, -9999.000,1.00500,    0,
1000.000,   0.00330,   0.00333,   0.00000,   0.00000,1.00000,1,  100.0,
9999.000, -9999.000,   1,1.0000
0 / END OF GENERATOR DATA, BEGIN BRANCH DATA
    1,    10,'1 ',   0.00000,   0.01470,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
    2,   -30,'1 ',   0.00000,   0.01470,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
   20,    30,'1 ',   0.00308,   0.04167,   0.00000,    0.00,    0.00,
0.00,,,  0.00000,  0.00000,  0.00000,  0.00000,1,   0.00,   1,1.0000
0 / END OF BRANCH DATA, BEGIN TRANSFORMER ADJUSTMENT DATA
0 / END OF TRANSFORMER ADJUSTMENT DATA, BEGIN AREA DATA
0 / END OF AREA DATA, BEGIN TWO-TERMINAL DC DATA
  1,2,    0.4000,   3930.00,    140.00,      0.00,    0.4000,   0.10000,'R',
0.00,  20,   1.00000
   10, 2,-5.70,-5.70, 0.0001, 1.1180,
500.0,0.10360,0.99495,1.11000,0.98000,0.00000,    0,    0,    0,'1 ', 3.7305
   20, 2,21.70,21.70, 0.0001, 1.3660,
525.0,0.09866,1.00857,1.11000,0.90000,0.00000,    0,    0,    0,'1 ', 6.3418
  2,2,    0.4000,   3930.00,    140.00,      0.00,    0.4000,   0.10000,'R',
0.00,  20,   1.00000
   10, 2,-5.70,-5.70, 0.0001, 1.1180,
500.0,0.10360,0.99495,1.11000,0.98000,0.00000,    0,    0,    0,'1 ', 3.7305
   20, 2,21.70,21.70, 0.0001, 1.3660,
525.0,0.09866,1.00857,1.11000,0.90000,0.00000,    0,    0,    0,'1 ', 6.3418
0 / END OF TWO-TERMINAL DC DATA, BEGIN SWITCHED SHUNT DATA
   10,0,1.00000,1.00000,    0,  170.00, 1, 170.00
   20,0,1.00000,1.00000,    0,  441.00, 1, 441.00
   30,0,1.00000,1.00000,    0,  249.00, 1, 249.00
0 / END OF SWITCHED SHUNT DATA, BEGIN IMPEDANCE CORRECTION DATA
0 / END OF IMPEDANCE CORRECTION DATA, BEGIN MULTI-TERMINAL DC DATA
0 / END OF MULTI-TERMINAL DC DATA, BEGIN MULTI-SECTION LINE DATA
0 / END OF MULTI-SECTION LINE DATA, BEGIN ZONE DATA
0 / END OF ZONE DATA, BEGIN INTER-AREA TRANSFER DATA
0 / END OF INTER-AREA TRANSFER DATA, BEGIN OWNER DATA
0 / END OF OWNER DATA, BEGIN FACTS CONTROL DEVICE DATA
0 / END OF FACTS CONTROL DEVICE DATA
```

13.3 Dynamic Model Setup

The nominal values of each block are,

IDN = 3930 A

UDN = 140 kV

Ls = 100 mH smoothing reactor

13.4 Dynamic Model Data File

```
1, 'GENCLS', 1, 0.0, 0.0 /  Update 990701
2, 'GENCLS', 1, 0.0, 0.0 /
1  'USRMDL'  0 'CDCAB2' 7 1
                      10 44 30 100
                      1 0 0 0 0 0 0 0 3 2
                      4.02
                      140.0  3.930
                      50.00  0  60.0  0  0  0
                      0 0 0 0 0 0 0 0
                      100
                      0 0 0 0 0 0
                      0.005 0.06  0.8 0.2 0.1 2.0 0.3
                      0.005 0.055 0.8 0.2 0.1 2.0 0.3
                       80.0 0.0005 40.0 0.0004
                       0 0/
2  'USRMDL'  0 'CDCAB2' 7 1
                      10 44 30 100
                      1 0 0 0 0 0 0 0 3 2
                      4.02
                      140.0  3.930
                      50.00  0  60.0  0  0  0
                      0 0 0 0 0 0 0 0
                      100
                      0 0 0 0 0 0
                      0.005 0.06  0.8 0.2 0.1 2.0 0.3
                      0.005 0.055 0.8 0.2 0.1 2.0 0.3
                       80.0 0.0005 40.0 0.0004
                       0 0/
/
```

13.5 Response File

14.5.1 Solve Load Flow

See paragraph 13.1.5.

14.5.2 Snap

See paragraph 13.1.5.

14.5.3 Start of dynamic simulation

Example of a response file to start dynamic simulation.

```
MENU,OFF      /* FORCE MENU TO CORRECT STATUS
```

```
RSTR
snap_btb.snp
LOFL
CASE
flow_btb.SAV
RTRN,FACT
CHAN
, , ,
13
10
20

20
5,'Idc1_r'
7,'Udc1_r'
35,'Idc2_r'
37,'Udc2_r'

0
STRT
start.out
0
RUN
0.0000,1,1,0
RUN
0.10000,10,10,0
ALTR
6
N
Y
,,0.00010000,,,
N
N
0
0
```

14.5.4 Run a -10% step in current order in both blocks

See paragraph 13.1.5

14.5.5 Plot a 10% step in current order

See paragraph 13.1.5

14 DATA SHEET

14.1 Dynamic data file single block dc transmission,

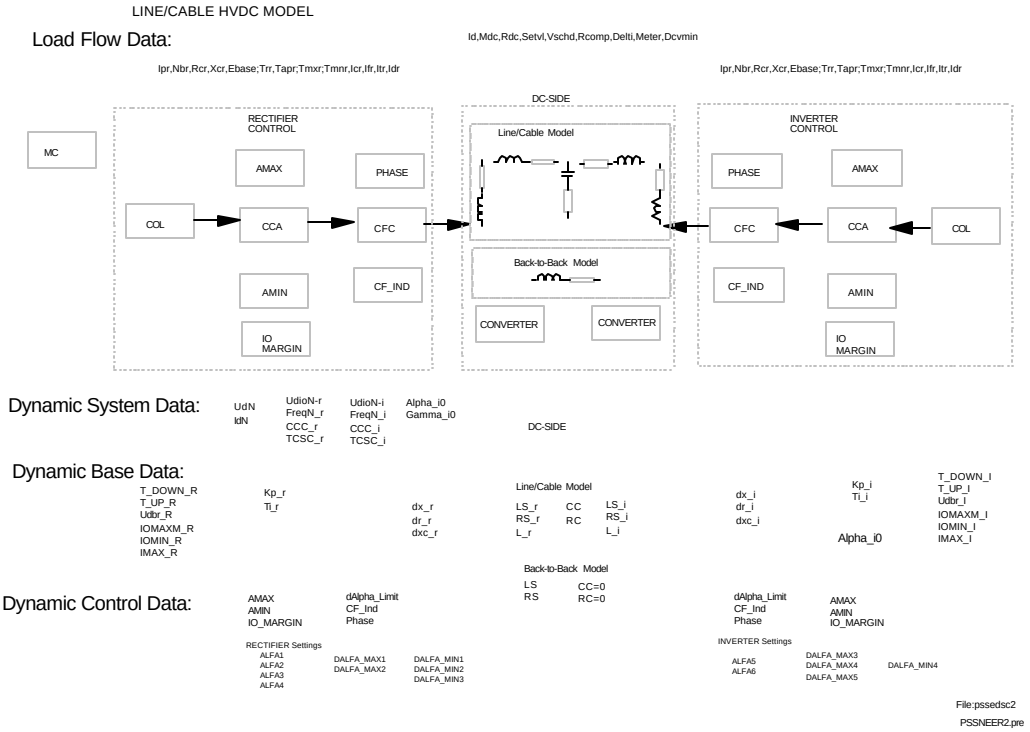
PTI POWER SYSTEM SIMULATOR

CDCAB2 (HVDC Transmission)

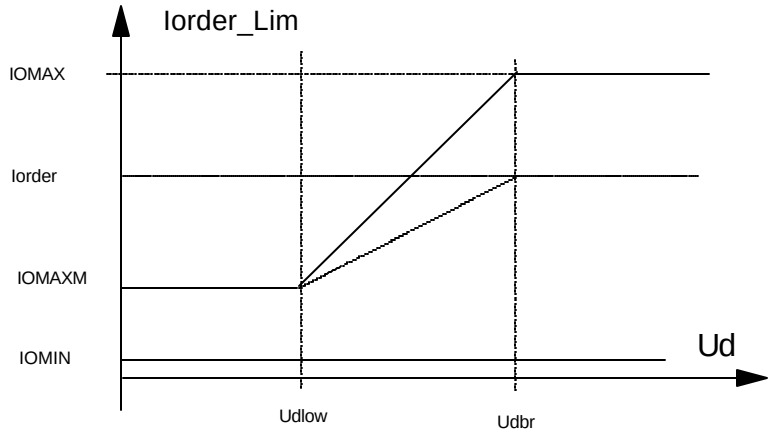
CALL CDCAB2(7,1,10,44,30,100) from CONEC
CALL TDCAB2(7,1,10,44,30,100) from CONET

This is HVDC model, Id #_____1_____ I,

using ICONs starting at #_____1_____ M,
and CONs starting at #_____5_____J,
and STATEs starting at #_____5_____K,
and VARs starting at #_____1_____L.



VOLTAGE DEPENDENT
CURRENT ORDER LIMITER



CONSTANTS

ICONs	#	Value	Description
M	1	1	Current direction, current from rect=1, inv=0
M+1		0	Block, internal program variable
M+2		0	Bypass rectifier, internal program variable
M+3		0	Bypass inverter, internal program variable
M+4		0	Frequency Control, disable=0 rectifier enable=1, inverter enabl = 2
M+5		0	Damping Controller, disable=0 rectifier enable=1,inverter enabl = 2
M+6		0	Internal program variable
M+7		0	Internal program variable
M+8		3	Internal program variable, CCC_Indication Rect=1,Inv=2,Rect+Inv=3
M+9		2	Internal program variable, Transmission Type Line/Cable=1, Back-to-Back=2

CONSTANTS

CONs	#	Value	NAME	DESCRIPTION
J	5	4.02	Iomax_Master	Max Limit in transmitted dc current, kA
J+1		280	UdN	Nominal DC Voltage in kV
J+2		3.93	IdN	Nominal DC Current in kA
J+3		50	Freq_Nom_r	Frequency at Rectifier, Hz
J+4		0©	CCC_ind_r	CCC indication Rectifier, CCC conv. CCC=1
J+5		60	Freq_Nom_i	Frequency at Inverter, Hz
J+6		0©	CCC_ind_i	CCC indication Inverter, CCC conv. CCC=1
J+7		0©	Alpha_r0	Delay angle init value rectifier (from Matlab)
J+8		0©	Alpha_i0	Delay angle init value inverter (from Matlab)
				Line/Cable Model
J+9		0	LS_r	Rectifier smoothing reactor inductance (mH)
J+10		0	RS_r	Rectifier smoothing reactor resistance (Ohm))
J+11		0	L_r	Rectifier line/cable inductance (mH)
J+12		0	CC	Linie/Cable capacitance (uF)
J+13		0	RC	Linie/Cable serie capacitance (Ohm)
J+14		0	LS_i	Inverter smoothing reactor inductance (mH)
J+15		0	RS_i	Inverter smoothing reactor resistance (Ohm))
J+16		0	L_i	Inverter line/cable inductance (mH)
				Back-to-Back Model
J+17		200	L_S	Smoothing reactor inductance (mH)
				Rectifier Converter
J+18		0©	dx_r	Commutation inductance,Transformer inductance
J+19		0©	dr_r	Commutation resistance,Transformer resistance
J+20		0©	dxc_r	Commutation capacitance
				Inverter Converter
J+21		0©	dx_i	Commutation inductance,Transformer inductance
J+22		0©	dr_i	Commutation resistance,Transformer resistance
J+23		0©	dxc_i	Commutation capacitance, inverter
				VDCOL Parameters, see Figure 1
J+24		0.005	T_Down_r	Time constant for decreasing dc voltage
J+25		0.06	T_Up_r	Time constant for increasing dc voltage
J+26		0.8	Udbr_r	Voltage breakpoint for activating VDCOL limit
J+27		0.2	Iomaxm_r	Maximum of lower VDCOL current limit
J+28		0.1	Iomin_r	Minimum of lower VDCOL current limit
J+29		2.0	Imax_r	Maximum Current limit of VDCOL
J+30		0.3	Udlow_r	Low breakpoint in dc voltage
J+31		0.002	T_Down_i	Time constant for decreasing dc voltage
J+32		0.055	T_Up_i	Time constant for increasing dc voltage
J+33		0.8	Udbr_i	Voltage breakpoint for activating VDCOL limit
J+34		0.2	Iomaxm_i	Maximum of lower VDCOL current limit
J+35		0.1	Iomin_i	Minimum of lower VDCOL current limit

J+36		2.0	Imax_i	Maximum Current limit of VDCOL
J+37		0.3	Udlow_i	Lower breakpoint in dc voltage
				CCA Parameters
J+38		80	Kp_r	CCA Rectifier,Proportional gain (deg/pu)
J+39		0.0005	Ti_r	CCA Rectifier,Integrator gain (deg/pu/sec)
J+40		40	Kp_i	CCA Inverter,Proportional gain (deg/pu)
J+41		0.0004	Ti_i	CCA InverterIntegrator gain (deg/pu/sec)
				Inverter control
J+42		0©	Gamp_ref_i	Inverter Gamma_prim reference (deg)
J+43		0		Spare Not used

Note: The symbol © indicates that the actual constant, if set to zero, is picked up from the load flow, otherwise the specified value are used.

STATE

STATEs	**#**	**DESCRIPTION**
K	5	DC Current, rectifier
K+1		DC Current measurement, rectifier
K+2		DC Voltage measurement, rectifier
K+3		DC Current, inverter
K+4		DC Current measurement, inverter
K+5		DC Voltage measurement, inverter
K+6		Cable voltage, not used in Back-to-Back
K+7		VDCOL dc voltage measuring, rectifier
K+8		VDCOL dc voltage measuring, inverter
K+9		CCA, integrator part, rectifier
K+10		CCA, integrator part, inverter
K+11		Alpha in rectifier
K+12		Alpha in inverter
K+13		Inverter current margin
K+14		Amin, rate of change
K+15		
K+16		Amax, rate of change
K+17		Amax current controller
K+18		Udio filter in Amax calculation
K+19		Not used
K+20		Commutation voltage
K+21		Frequency measuring in rectifier
K+22		Frequency measuring in rectifier
K+23		Damping Controller filter 1
K+24		Damping Controller filter 2
K+25		Master control, dc voltage measuring
K+26		Alpha filtering, rectifier

K+27		Alpha filtering, inverter
K+28		Not used
K+29		Not used

VARIABLES:

VARs	#	Value	NAME	DESCRIPTION
L	1		Pac_r	Active power in rectifier
L+1			Qac_r	Reactive power in rectifier
L+2			Pac_i	Active power in inverter
L+3			Qac_i	Reactive power in inverter
L+4			Ioo	MC; DC current order
L+5			Iorder_r	VDCOL, limited dc current order, rectifier
L+6			Iorder_i	VDCOL, limited dc current order, inverter
L+7			I_error_r	CCA, current control error, rectifier
L+8			Aprop_r	CCA, proportional part, rectifier
L+9			Alfa_order_r	CCA, alpha order, rectifier
L+10			Amin_cca_r	Alpha minimum limit, rectifier
L+11			Amax_cca_r	Alpha maximum limit, rectifier
L+12			I_error_i	CCA, current control error, inverterr
L+13			Aprop_i	CCA, proportional part, inverter
L+14			Alfa_order_i	CCA, current control error, inverter
L+15			Amin_cca_i	Alpha minimum limit, inverter
L+16			Amax_cca_i	Alpha maximum limit, inverter
L+17			Alpha_r	CFC, Alpha rectifier
L+18			Alpha_i	CFC Alpha inverter
L+19			dang_r	Phase shift correction
L+20			dang_i	Phase shift correction
L+21			Us_kv_r	Converter voltage, rectifier
L+22			Us_kv_i	Converter voltage, rectifier
L+23			Udc_r	DC voltage, rectifier
L+24			Udc_i	DC voltage, inverte
L+25			Id_r	DC current, rectifier
L+26			Id_i	DC current, inverter
L+27			Alfa_r	Alpha, rectifier
L+28			Alfap_r	Alphaprim, rectifier
L+29			Alfa_i	Alpha, inverter
L+30			Gama_i	Gamma angle, inverter
L+31			Gamap_i	Gamma prim angle, inverter
L+32			abs(Iac_r)	Injected ac current, rectifier
L+33			abs(Iac_i)	Injected ac current, inverter
L+34			Us_r	DC voltage, rectifier
L+35			Us_i	DC voltage, inverter
L+36			Delt_Po_Freq	FC, Frequency modulation
L+37			Delt_Po_Stab	DC, Damping Control modulation
L+38			Inv_Io_Margin	Inverter current order margin
L+39-99			Test	Storage of internal program variables

14.2 Dynamic data file double block dc transmission

PTI POWER SYSTEM SIMULATOR

CDCAB2
(HVDC Transmission)

CALL CDCAB2(7,1,10,44,30,100) from CONEC
CALL TDCAB2(7,1,10,44,30,100) from CONET

This is HVDC model, Id #_____1____ I,

using ICONs starting at #_____1____ M,
and CONs starting at #_____5_____J,
and STATEs starting at #_____5_____K,
and VARs starting at #_____1_____L.

CONSTANTS

CONs	#	Value	NAME	DESCRIPTION
J	5	4.5	Iomax_Master	Max Limit in transmitted dc current, kA
J+1		140	UdN	Nominal DC Voltage in kV
J+2		3.93	IdN	Nominal DC Current in kA
J+3		50	Freq_Nom_r	Frequency at Rectifier, Hz
J+4		0	CCC_ind_r	CCC indication Rectifier, CCC conv. CCC=1
J+5		60	Freq_Nom_i	Frequency at Inverter, Hz
J+6		0	CCC_ind_i	CCC indication Inverter, CCC conv. CCC=1
J+7		0	Alpha_r0	Delay angle init value rectifier (from Matlab)
J+8		0	Alpha_i0	Delay angle init value inverter (from Matlab)

Data list continues as in 15.1.

PTI POWER SYSTEM SIMULATOR

CDCAB2
(HVDC Transmission)

CALL CDCAB2(7,1,10,44,30,100) from CONEC
CALL TDCAB2(7,1,10,44,30,100) from CONET

This is HVDC model, Id #_____2_____ I,

using ICONs starting at #_____11_____ M,
and CONs starting at #_____49_____J,
and STATEs starting at #_____35_____K,
and VARs starting at #_____101_____L.

CONSTANTS

CONs	#	Value	NAME	DESCRIPTION
J	49	4.5	Iomax_Master	Max Limit in transmitted dc current, kA
J+1		140	UdN	Nominal DC Voltage in kV
J+2		3.93	IdN	Nominal DC Current in kA
J+3		50	Freq_Nom_r	Frequency at Rectifier, Hz
J+4		0	CCC_ind_r	CCC indication Rectifier, CCC conv. CCC=1
J+5		60	Freq_Nom_i	Frequency at Inverter, Hz
J+6		0	CCC_ind_i	CCC indication Inverter, CCC conv. CCC=1
J+7		0	Alpha_r0	Delay angle init value rectifier (from Matlab)
J+8		0	Alpha_i0	Delay angle init value inverter (from Matlab)

Data list continues as in 15.1.

14.3 DATA FILE

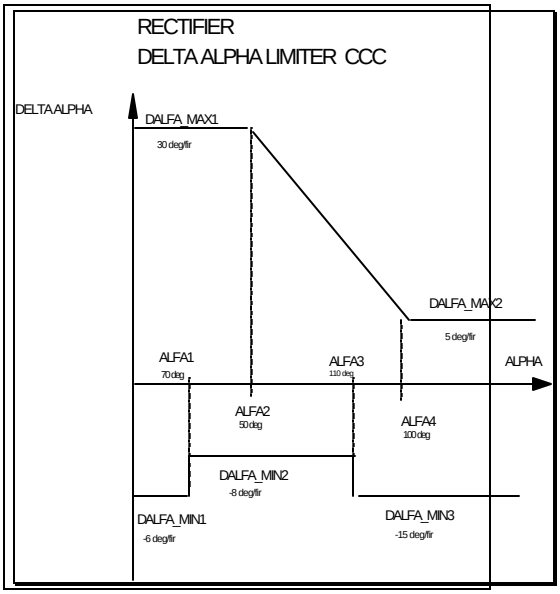
```
C /*----------      LIBRARY VERSION PSS/E    ----------*/
C  *
C  *                  Name      : DATA_BTB_926.f
C  *                  Function  : CONSTANT SETTING
C  *                     XN 649 062
C  *                  Revision  : 990315,990630
C  *---------------------------------------------------------------------
C COPYRIGHT ABB POWER SYSTEMS HVDC SWEDEN
C This document must not be copied without our written permission,
C and the contents thereof must not be imparted to a third party
C nor be used for any unauthorized purpose. Contravention will be
C prosecuted.
C  * ---------------------------------------------------------------------
C
C
      SUBROUTINE  SET_CONSTANTS_926(ID_HVDC)
C
      Integer ID_HVDC
C
C   DECLARATION OF PUBLIC VARIABLES IN COMMON MEMORY
C ****************************************************************
C    COMMON MEMORY OF CONSTANTS
C  ************************************
C
       Include 'cfc_constants_926.ins'
C
C  --  Max Calculation step without internal integration
C
        DELTMAX  =  0.5000000E-03
C
C  --- HVDC Back To Back System Paramerer:
C
C  --  Line/Cable HVDC System Paramerer:
C
C  --- DC Side Components:  ----------
C
C  --- Frequency Controller  -----
       Kfc_prop = 1.0 ! Gain MW/Hz
       Kfc_der = 1.0 ! Gain MW/Hz
       Db_p      = 0.05     ! Dead Band prop
       Db_d      = 0.05     ! Dead Band der.
       Tfc_meas  = 0.1   ! Measuring filter
       Tfc_der =  1.0     ! Der. filter
C  --- Damping Controller  ------
       Tdamp_1 = 0.1
       Tdamp_2 = 1.0
       Damp_Gain = -100.
       Damp_Max =  50.
       Damp_Min = -50.
C  --  Master Controller  ------
       Ud_ref_mc = 0.8  ! Ref voltage pu
       Ud_ref_min= 0.8
       Tud_Mc_hi = 1.0   ! 1 sec
       Tud_Mc_low = 0.1  ! 100 ms
C
C  External Constants
C IOMAX_MASTER:
C UdN:
C IdN:
C Freq_Nom_r
C CCC_ind_r
C
C Freq_Nom_i
C CCC_ind_ri
C
        pi = acos(-1.0)
        to_rad = pi / 180.0
C
C  --- CCA Current Control Amplifier:
         A_MAX_R  =   164.1640 * to_rad    ! deg
```

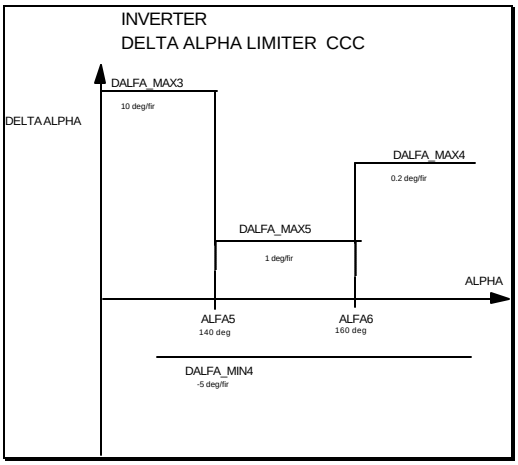
```
      A_MIN_R =  5.000000 * to_rad     ! deg
      A_NOM_R =  17.50000 * to_rad     ! deg
      LIN_MAX_R =  1.000000
      LIN_MIN_R =  0.3000000
C --- Kp_R =  20.00000  * to_rad    ! deg/pu Id
C 971106---       Ti_r =  5.0000002E-04 /  to_rad !  sec
      APROP_MAX_R =  180.0000  * to_rad    ! deg
      APROP_MIN_R =  -180.0000  * to_rad    ! deg
      A_MAX_I =  164.0000 * to_rad     ! deg
      A_MIN_I =  5.000000 * to_rad     ! deg
      A_NOM_I =  17.50000  * to_rad    ! deg
      LIN_MAX_I =  1.000000
      LIN_MIN_I =  0.3000000
      APROP_MAX_I =  180.0000  * to_rad    ! deg
      APROP_MIN_I =  -180.0000  * to_rad    ! deg
C --- CCA Current Control Integrator:
      AINT_MAX_R =  165.0000  * to_rad    ! deg
      AINT_MIN_R =  5.000000  * to_rad    ! deg
      AINT_MIN_I =  105.0000  * to_rad    ! deg
      AORDER_MIN_R =  5.000000 * to_rad     ! deg
      AORDER_MIN_I =  105.0000  * to_rad    ! deg
C ---       CFC Delta Alpha Limiter:
      T_CFC_R =  1000.000
      ALFA_MAX_R =  180.0000  * to_rad    ! deg
      T_CFC_I =  1000.000
      ALFA_MIN_I =  110.0000  * to_rad    ! deg
      ALFA1 =  70.00000 * to_rad     ! deg
      ALFA2 =  50.00000 * to_rad     ! deg
      ALFA3 =  110.0000  * to_rad    ! deg
      ALFA4 =  100.0000 * to_rad     ! deg
      ALFA5 =  140.0000 * to_rad     ! deg
      ALFA6 =  160.0000  * to_rad    ! deg
      DALFA_MAX1 =  30.00000 * to_rad     ! deg
      DALFA_MAX2 =  5.000000 * to_rad     ! deg
      DALFA_MAX3 =  10.00000 * to_rad     ! deg
C 980513 DALFA_MAX4 =  0.2000000  * to_rad    ! deg
      DALFA_MAX4 =  5.2000000  * to_rad    ! deg
      DALFA_MAX5 =  1.000000  * to_rad    ! deg
      DALFA_MIN1 =  -6.000000  * to_rad    ! deg
      DALFA_MIN2 =  -8.000000  * to_rad    ! deg
      DALFA_MIN3 =  -15.00000  * to_rad    ! deg
      DALFA_MIN4 =  -5.000000  * to_rad    ! deg
      TANG_R =  5.0000001E-02
      TANG_I =  5.0000001E-02
C  --- VDCOL Current Order Limiter:
C --- Current/Voltage Measuring:
      TIDC_R =  2.0000001E-03
      TVDC_R =  1.0000000E-03
      TIDC_I =  2.0000001E-03
      TVDC_I =  1.0000000E-03
C --- Alpha  Measuring:
      Tcr =  3.0000000E-03
      Tci =  3.0000000E-03
C --- DC Side Components:
C --- Converter Bypass Ref.in AC Level:
      VAC_BYP_I =  11.00000 !   kV
      VAC_UNBYP_I =  18.00000 !   kV
      IdNx =  1.500000      ! Not used
      CURMARG =  2.0000000E-02   ! Not used
C --- Conv.Conv.Parameters not used
      MANBYP_R =  0.0000000E+00
      MANBYP_I =  0.0000000E+00
      GAMMINNOM_R =  17.00000 * to_rad    ! deg
      GAMMINNOM_I =  17.00000 * to_rad    ! deg
C --- Transient Controller Inverter:
C --- Gamma0 data:
      USGO = 0.4
      T1GO = 0.05     ! Time to activate, 980202
      URGO = 0.5
      T2GO = 0.0
      UDGO = 0.35
      DAGO = 1.75
C --- Converter dx & dr:
C --- Additional step in Current Order:
```

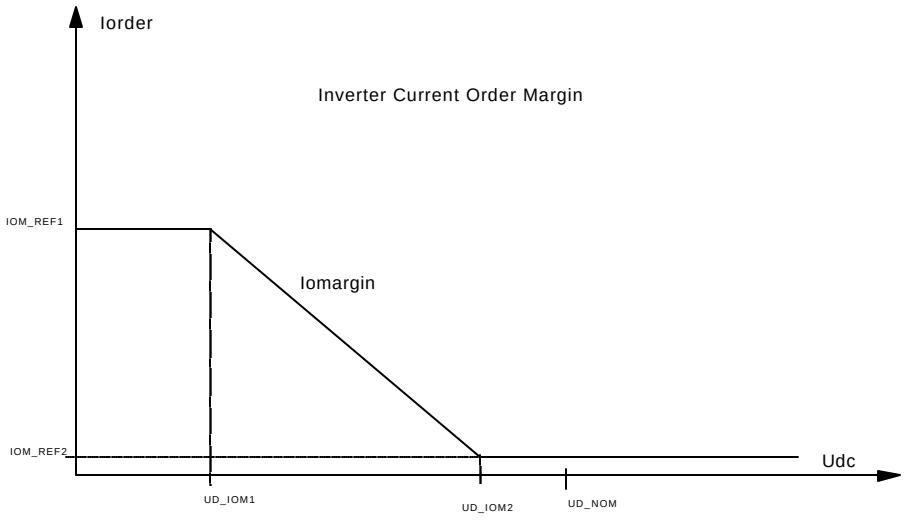
```
      DIorder =  0.0000000E+00
      Tf_r =  0.0000000E+00
      Tf_i =  0.0000000E+00
      Tof_r =  9.9999998E-03
      Tof_i =  9.9999998E-03
C  --- Dynamic Current Compounding:
C  --- Transient Controller Rectifier:
      ultrpu = 0.50
      datr  = 40.0 * to_rad
      dbtr  = 40.0 * to_rad
      t1tr  = 0.02
      t2tr  = 0.01
      t3tr  = 0.01
      t4tr  = 0.125
C  --- Commutation Failure Inverter:'
      Tf_cf_ccc  = 0.1
! 980513 Ucf_ref_ccc = 0.2 Increase to
      Ucf_ref_ccc = 0.4
      Tcf_ccc  = 0.025
      Tf_cf_lcc  = 0.1
      Ucf_ref_lcc  =0.1
      Tcf_lcc  = 0.050
C *** New CCC Constants ***
C  --  Voltage Dependent Current Margin
      IOM_Tc_Ud_Down = 0.012
      IOM_Tc_Ud_Up  = 0.010
      UD_IOM1  = 0.5
      UD_IOM2  = 0.93
      IOM_Ref1 = 0.90
C 971105       IOM_Ref2 = 0.02
      IOM_Ref2 = 0.03
C  --- Alpha Min Parameters:
C 971008 U_vfir_min =  9.1300003E-02
      U_vfir_min =  8.7100003E-02
      G0_r =  -4.7269999E-03
      G1_r =  1.770110
      G2_r =  0.1520610
C  --- Alpha Max Parameters:
      K0_r =  -1.8846501E-02 * to_rad  ! deg
      K1_r =  106.2090  * to_rad    ! deg
      K2_r =  9.377900 * to_rad    ! deg
       Kgp0_r =  0.0000000E+00 * to_rad  ! deg
      Kgp1_r =  -0.6012880 * to_rad    ! deg
      Kgp2_r =  -2.9795799E-02 * to_rad  ! deg
      Gamp_ref_r =  17.00000 * to_rad    ! deg
      Gamp_min_r =  15.00000 * to_rad    ! deg
C 980514 Amin_udr =  -9.876990 * to_rad    ! deg
      Amin_udr =  -14.1 * to_rad    ! deg
       K0_i =  -1.8846501E-02 * to_rad  ! deg
       K1_i =  106.2090  * to_rad    ! deg
       K2_i =  9.37790  * to_rad    ! deg
      Kgp0_i =  0.0000000E+00 * to_rad  ! deg
      Kgp1_i =  -0.6012880  * to_rad    ! deg
      Kgp2_i =  -2.9795799E-02 * to_rad  ! Con(j+149), '  deg'
      Gamp_min_i =  15.00000 * to_rad   ! ',Con(j+151), '  deg'
C 990708 Garabi setting in Brazil
       Amax_udi =  200.0 * to_rad  ! ',Con(j+152)
C
C  ---------------------------------------
      Plot_on = 0.0 ! Write to X-window deactive
C       Plot_on = 1.0 ! Write to X-window active
C       Plot_on = 2.0 ! Write to X-window active
C       Plot_on = 3.0 ! Write to X-window active
C  ---------------------------------------
C
C  ************************************
C  MODIFY SYSTEM DATA OF SELECTED HVDC TRANSMISSIONS
C  ************************************
C      HVDC Identity Nr. 9 modify plot data
C
      IF (ID_HVDC.EQ.9) Then

       Plot_on = 0.0
```

```
      Endif
C -------------------------------------
      Return
      End
C
```







14.4 DYNAMIC MODEL INSTALLATION IN PSS/E Ver. 26

14.4.1 Background

The PSS/E program ver.26 should be installed according to the instruction in documentation of the program, see paragraph “PSS/E on the PC for “Windows NT and Windows 95”.

To be able to include the user-built dynamic HVDC model you need to install the Digital Visual Fortran 5.0 compiler. This ensure that the user model is compiled and linked with the same tools that were used to build the main PSSE.DLL file

The dynamic HVDC model is compiled by the Fortran-compiler outside the PSS/E program and the resulting object-file is linked together with the PSS/E into an executable file by using “CLOAD4.BAT” supplied by the PSS/E program.

At the compilation of the HVDC model Fortran-file, the declaration files of the actual program version must be possible to read. All the common variables are declared in this way. These declaration files are supplied with PSS/E program and the path must be setup at the installation of the program.

14.4.2 Installing the Dynamic HVDC/CCC Model

The two test cases are described in the beginning of this Appendix.

All the files should be placed to a working directory, one directory for each case. The test cases will then be ready to start. The operation procedure is simplified by using the response files,

solv_lf.idv

snap_btb.idv

strt_btb.idv

run_step.idv

plot_step.idv

Note, The identity of your printer has to be added into the plot-response-file (plot_step.idv).

The response files are included just to simplify the operation procedure and can be change at your own discretion.

Return to DOS-level and compile and link the object codes. This is performed by using following bat-files,

compile.bat (generated by the PSS/E command DYRE)

comp_926.bat

link_926.bat

The version number, 926, indicates the year of 1999 and version 26.

The test cases should be studied at first to get familiar with the operation procedure of this model and verify that the same result is obtained.

After that the model can be used in a more complex system.

The dynamic variables are stored in file “fort.99” at the command “DOCU”.

The result of the internal execution of the calculation is presented in a file: CCreport.txt. This option is switch off by default but can be activated by the parameter, Plot_on, in the data-file.

Appendix 2

15 QUICK START PROCEDURE FOR RUNNING ON PC

The following is a quick guide to get started using the Response files (*xxxx.idv*) provided. A listing of the *idv* files is provided in section 2.5.

Step 1. Run *solv_lf.idv*

1. Open the pss/e load flow program: select **IO Control** and then **Set dialog input device**, choose and execute *solv_lf.idv*. .
2. Exit pss/e load flow.

This will generate a solved load flow saved case, *flow_btb.sav*, using the raw data file *flow_btb.dat*.

Step 2. Run *snap_btb.idv*

1. Open the pss/e dynamic program: select **IO Control** and then **Set dialog input device**, choose and execute *snap_btbf.idv*. .

2. Exit pss/e dynamic program.

This will create a snap file, *snap_btb.snp*, that will be used for subsequent dynamic runs.

Step 3. Compile and Link

1. Get in DOS and the appropriate directory where the files for this case is located, execute the following commands in sequence:

compile
comp_926
link_926

2. Exit DOS.

3. Create a “short-cut” to start the pss/e dynamic program and modify the path so that the correct *dsusr.dll* file from the appropriate directory will be used.

Step 4. Run *strt_btb.idv*

1. Start the pss/e dynamic simulation using the “short-cut” created in Step 3 above.

2. Select **IO Control** and then **Set dialog input device**, choose and execute *strt_btb.idv*. .

This will initialize and set the case up ready for disturbance simulation. Quantities to be saved for plotting are entered by the execution of *strt_btb.idv.* The converter transformer tap position for the rectifier and inverter are also modified. Note that the time step size is specified in and by *strt_btb.idv*, and the output for plotting will be stored in the file *strt.out*.

The case is now ready for dynamic simulation. The following step is an example of a dynamic simulation case in which the dc current order is increased in a 10% step for 100 ms, and then decreased by a 10% step to return to the original value.

Step 5. Run *run_btb_step.idv*

1. Select **IO Control** and then **Set dialog input device**, choose and execute *run_btb_step.idv*. .

The current order is step increased and decreased. The results can be plotted by running the pss/e plot program. The user can also select and plot directly without following step 6.

Appendix 3

16 QUICK START PROCEDURE FOR RUNNING ON UNIX

The following is a quick guide to get started using the Response files (*xxxx.idv*) provided. A listing of the *idv* files is provided in section 2.5.

Step 1. Run *solv_lf.idv*

1. Open the pss/e load flow program (**psslf4**): select **IO Control** and then **Set dialog input device**, choose and execute *solv_lf.idv*. .
2. Exit pss/e load flow.

This will generate a solved load flow saved case, *flow_btb.sav*, using the raw data file *flow_btb.dat*.

Step 2. Run *snap_btb.idv*

1. Open the pss/e dynamic program (**pssds4**): select **IO Control** and then **Set dialog input device**, choose and execute *snap_btb.idv*. .

2. Exit pss/e dynamic program.

This will create a snap file, *snap_btb.snp*, which will be used for subsequent dynamic runs.

Step 3. Compile and Link

1. In the same directory where the files for this case are located, execute the following commands (unix version) in sequence:

chmod u+x compile
compile
comp_926
link_926

Step 4. Run *strt_btb.idv*

1. Start the pss/e dynamic simulation.

2. Select **IO Control** and then **Set dialog input device**, choose and execute *strt_btb.idv*. .

This will initialize and set the case up ready for disturbance simulation. Quantities to be saved for plotting are entered by the execution of *strt_btb.idv.* The converter transformer tap position for the rectifier and inverter are also modified. Note that the time step size is specified in and by *strt_btb.idv*, and the output for plotting will be stored in the file *strt.out*.

The case is now ready for dynamic simulation. The following step is an example of a dynamic simulation case in which the dc current order is increased in a 10% step for 100 ms, and then decreased by a 10% step to return to the original value.

Step 5. Run *run_btb_step.idv*

1. Select **IO Control** and then **Set dialog input device**, choose and execute *run_btb_step.idv*. .

The current order is step increased and decreased. The results can be plotted by running the pss/e plot program. The user can also select and plot directly without following step 6.